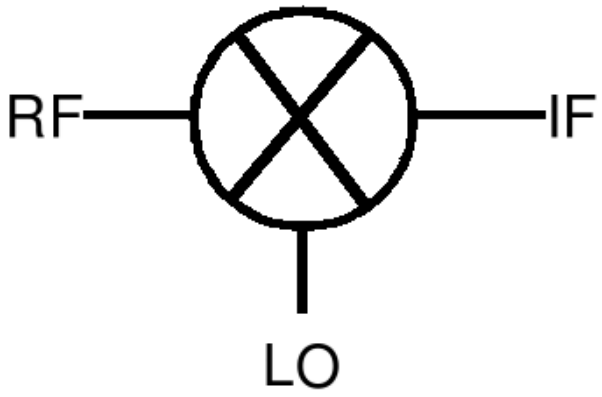
Project ENGN4545

- Mixers
- Radio Architectures
- Project description
- Frequency Synthesisers
- Introduction to the Radiofrequency chips used in the projects.

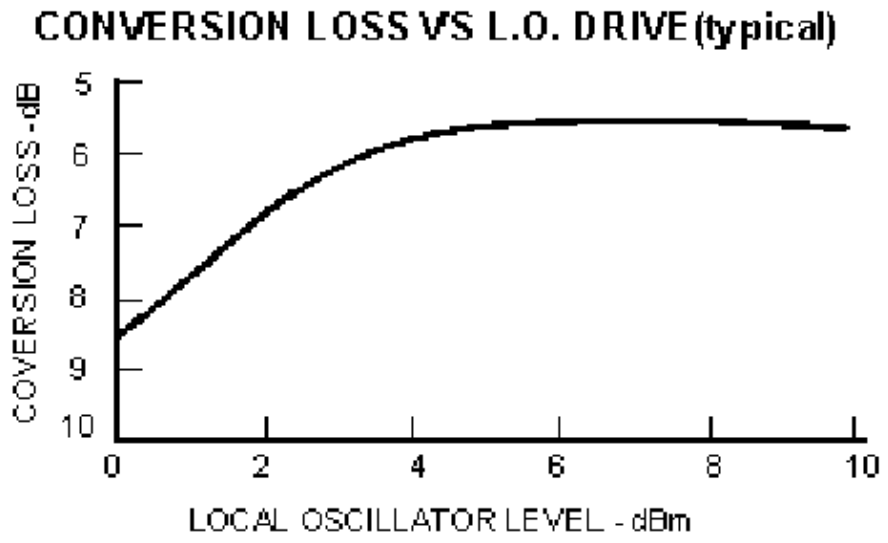
Mixers

- Mathematically, mixers are multipliers.
- Terminology in the following figure and loosely: $IF = RF \times LO$.
- Multiplication of sine waves produces sines waves of different frequencies (trig formulae).



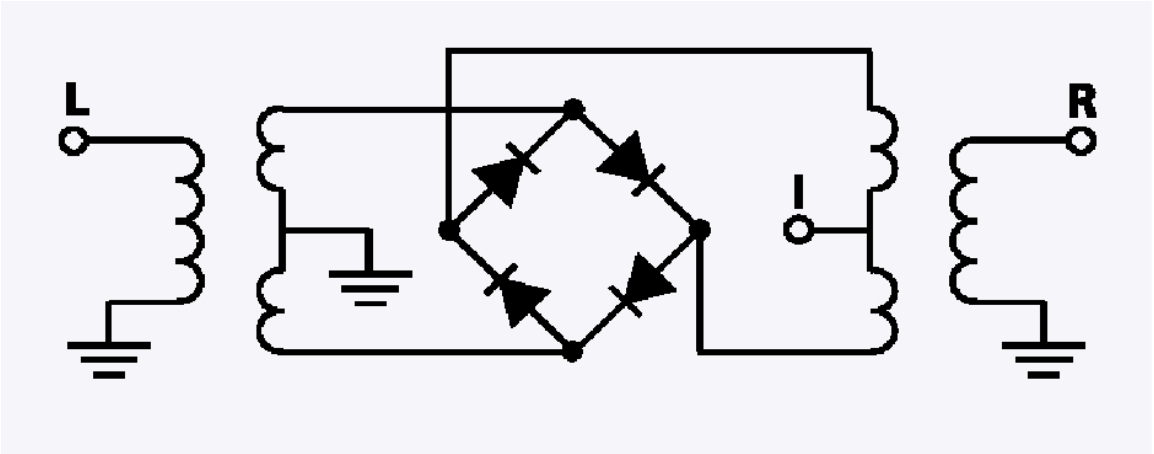
Mixers

- In practice most mixers are designed to be non linear on the LO port.
- Conversion loss or gain is the mixer transfer function.



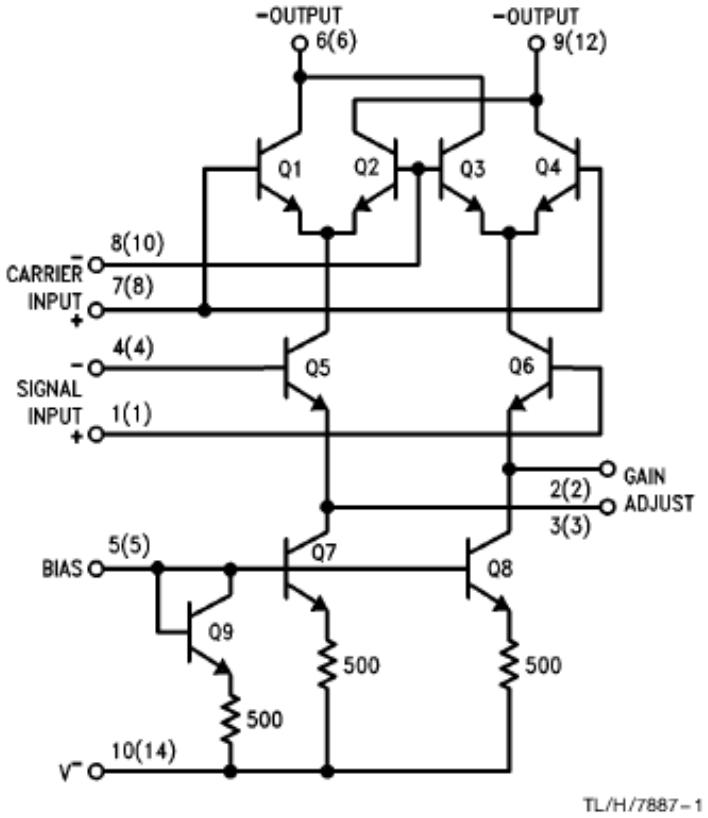
Balanced Diode Ring Modulator Demodulator

- Commonly used up to microwave frequencies.



LM1496 Balanced Modulator Demodulator

- VHF frequencies only.



Numbers in parentheses show DIP connections.

Superhet Transceiver

- Most popular design.
- Very sensitive.
- Problems with image frequencies.

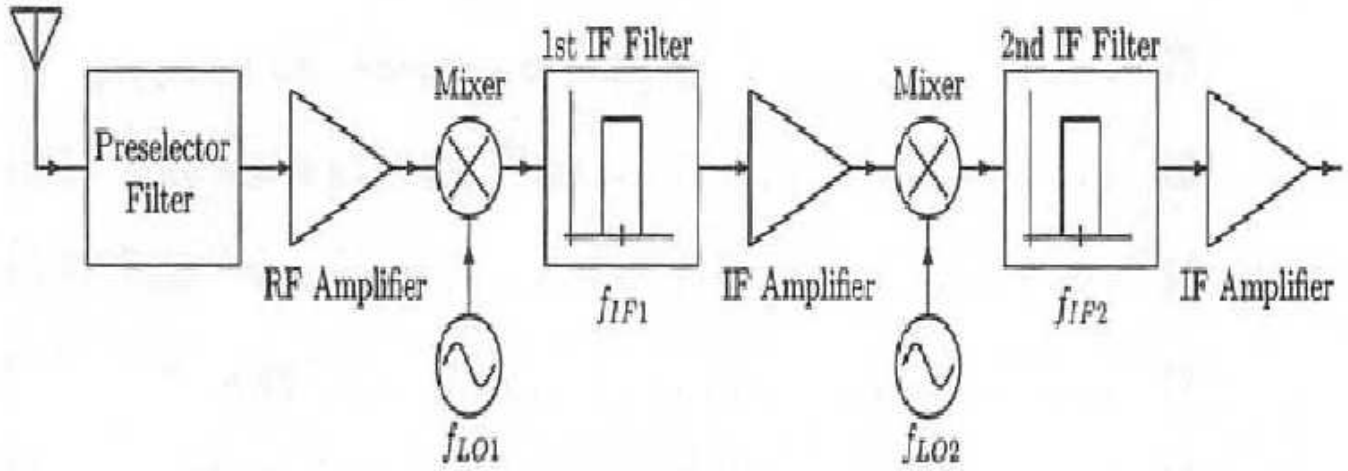
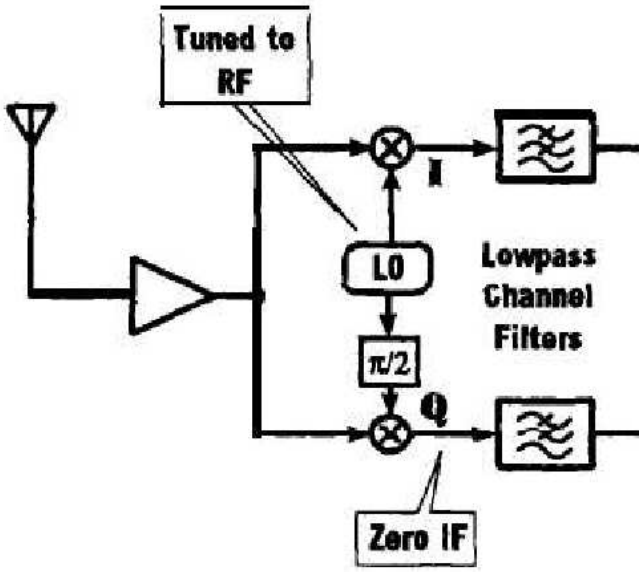


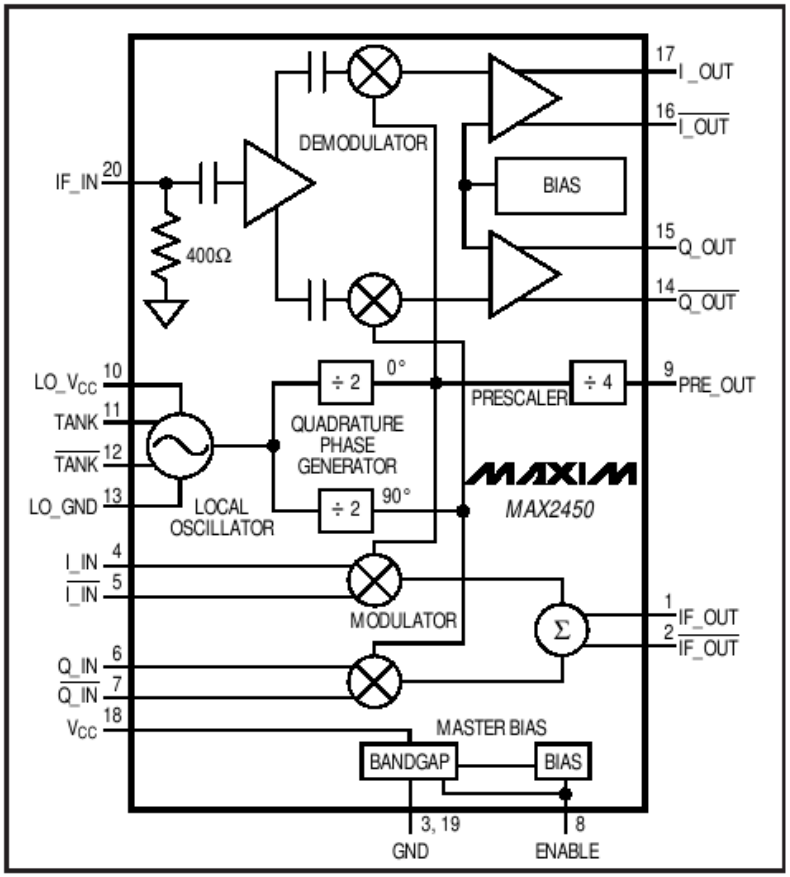
Figure 32: The Superheterodyne Receiver

Direct Conversion

- Becoming more popular due to simplicity of architecture.
- Sensitivity affected by baseband noise.
- No image frequency issues.
- Production of I and Q requires a 90^o phase shifter. Added complexity.
- Low frequency baseband can be digitised. (MAX2450).

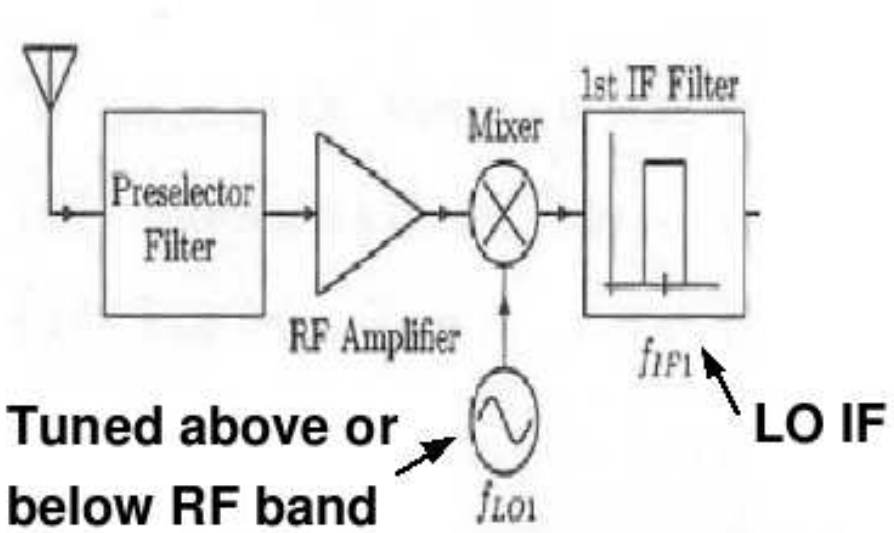


MAX2450 IQ Transceiver

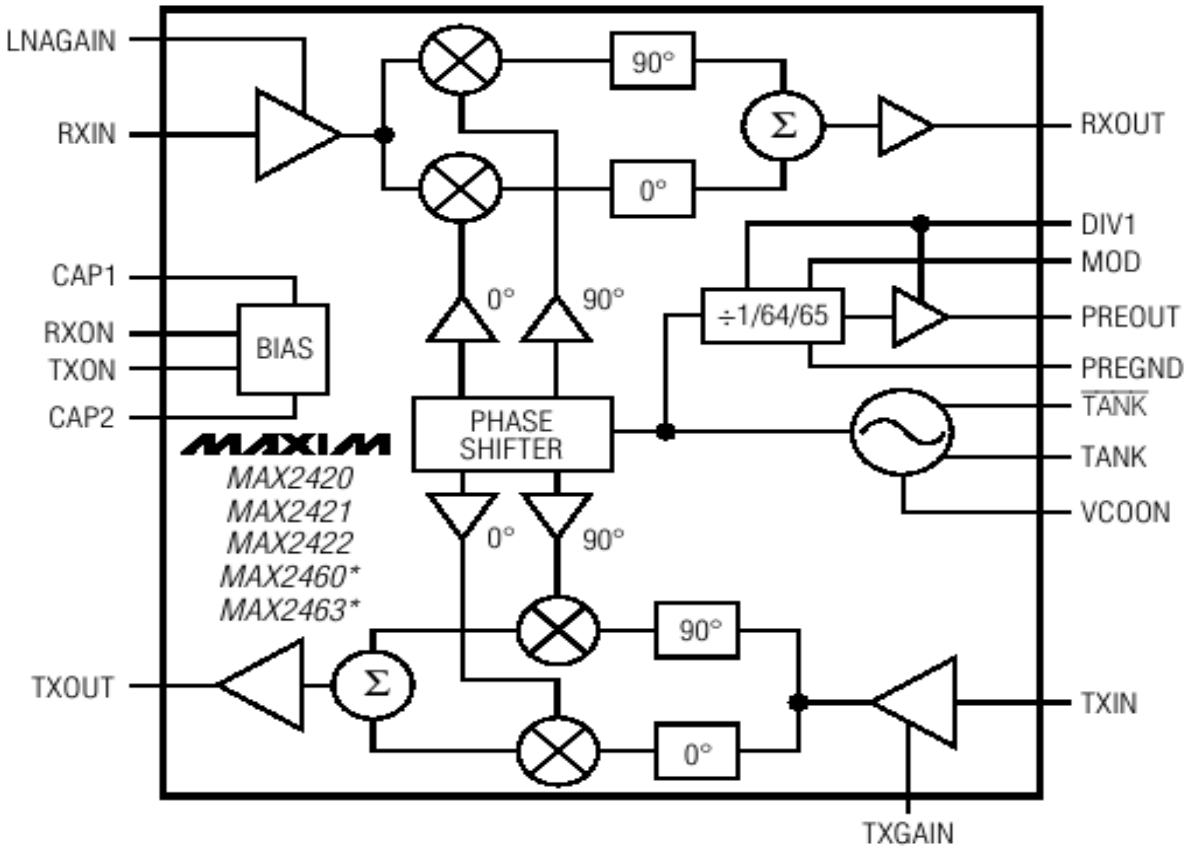


Low Intermediate Frequency Receiver

- Best of both worlds in Software Defined Radio because the LOW IF can be digitised and avoid the 90^o phase shifter.
- This is our approach. (Also MAX2420)
- Still has the image problem like all superhets.



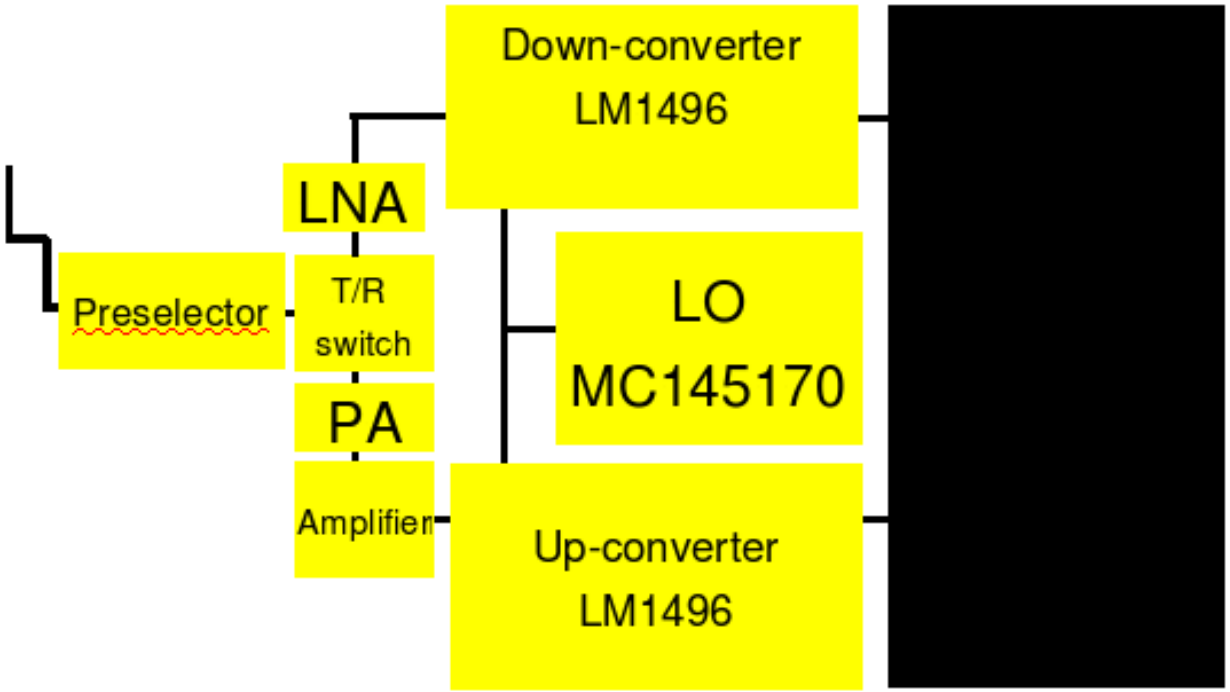
MAX2420 Image Reject Transceiver



ENGN4545 Project

- Two projects. A choice that depends on your skills and preferences.
- Transceiver 1. Based on the LM1496 balanced modulator/demodulator. Discrete design. Lots of practice in applying theory learnt in the course.
- Transceiver 2. Based on integrated solutions: AD9874 (IF digitising subsystem) as the receiver and the AD9854 (Direct digital synthesiser) as the transmitter.
- Work in pairs, collaborate as a class.

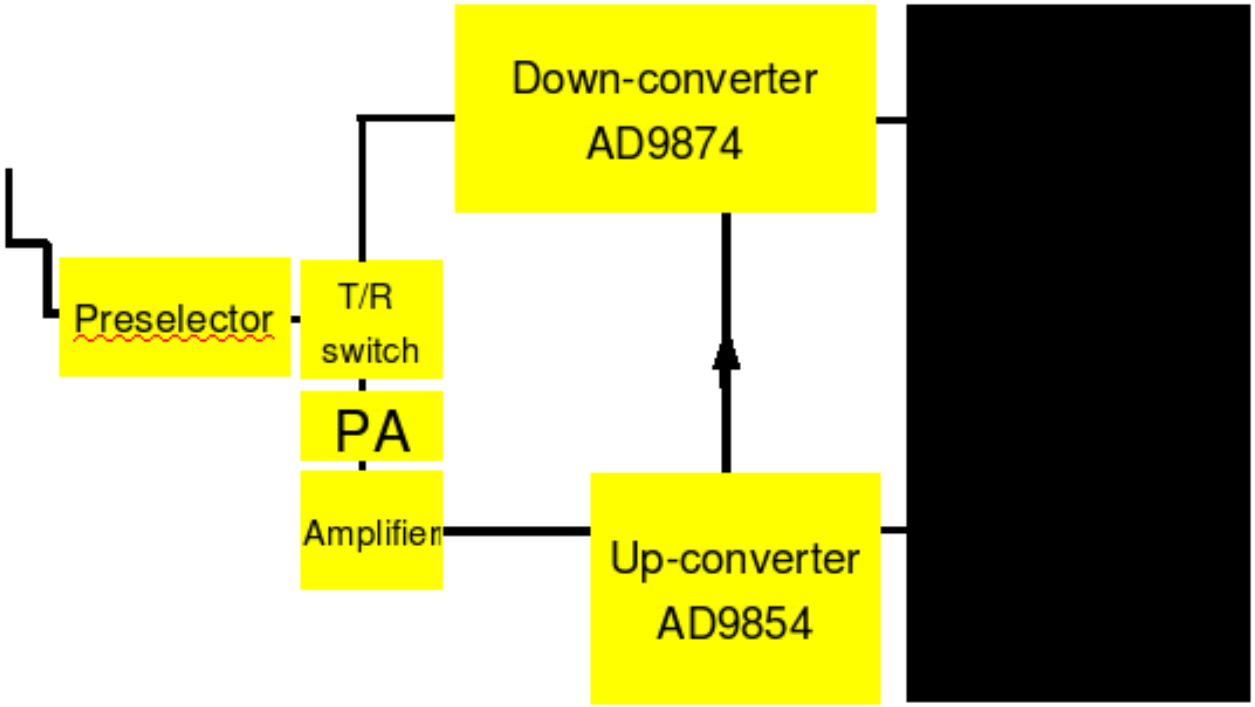
Transceiver 1



Transceiver 1

- Discrete. Design each sub-circuit.
- Easy to understand all the details and modify the design.
- Very flexible because it is a low IF down/up converter. Can handle any modulation scheme by leaving it to the baseband processor.
- Cheaper and faster in a one off.
- Easiest for those who understand the theoretical aspects of the course well and are good at RF design.
- Can do a breadboard dead-bug prototype to get working before you do the PCB. (Advisable)

Transceiver 2



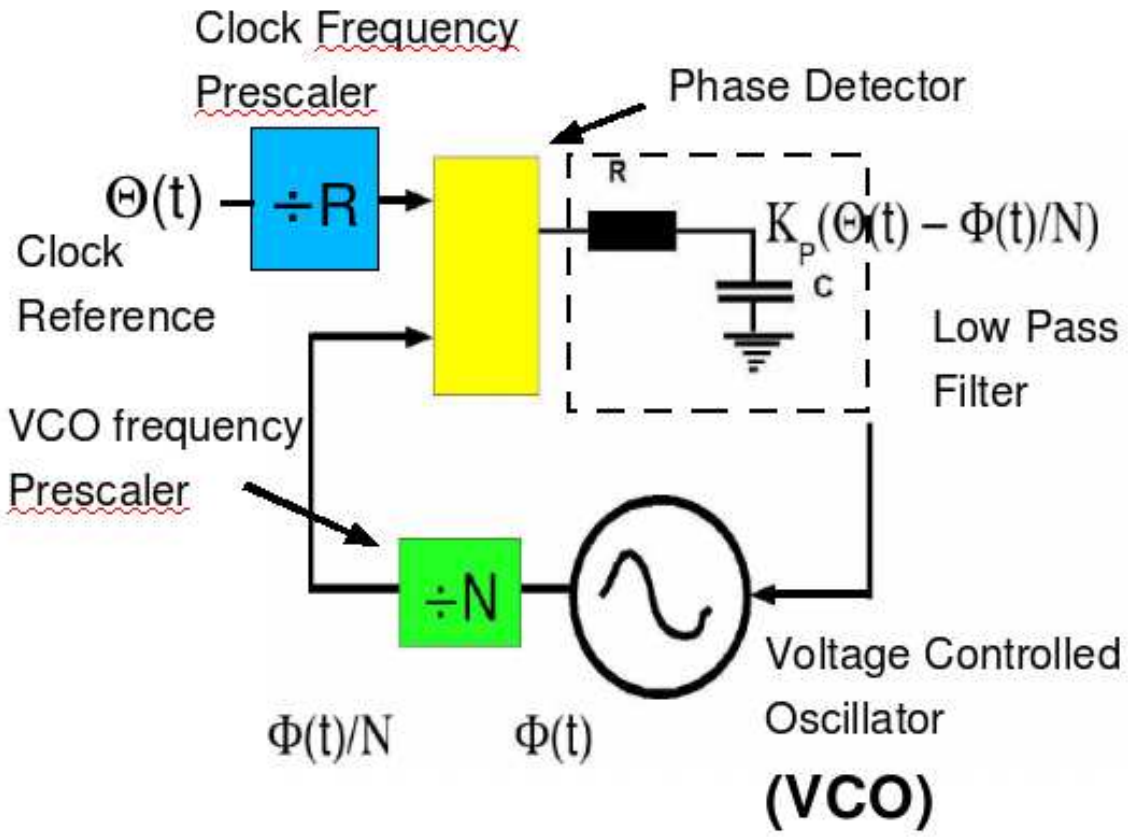
Transceiver 2

- Integrated. Plug-n-play.
- Need to read the datasheets for the AD9854 and AD9874 carefully.
- Also very flexible for the same reason.
- Cheaper and faster in the long run.
- Ideal for those who wish to experience state of the art and are good at RF PCB design and soldering.
- Cannot do a breadboard dead-bug prototype. Start with a PCB layout. I.E. start EAGLE (or whatever) design immediately.

Frequency Synthesisers

- Provide the source of the Radiofrequency carrier signals
- Two types of circuit used...
- Phase lock loop (PLL) and voltage controlled oscillator (VCO)
- Direct Digital Synthesiser (DDS).

Phase Lock Loop and Voltage Controlled Oscillator



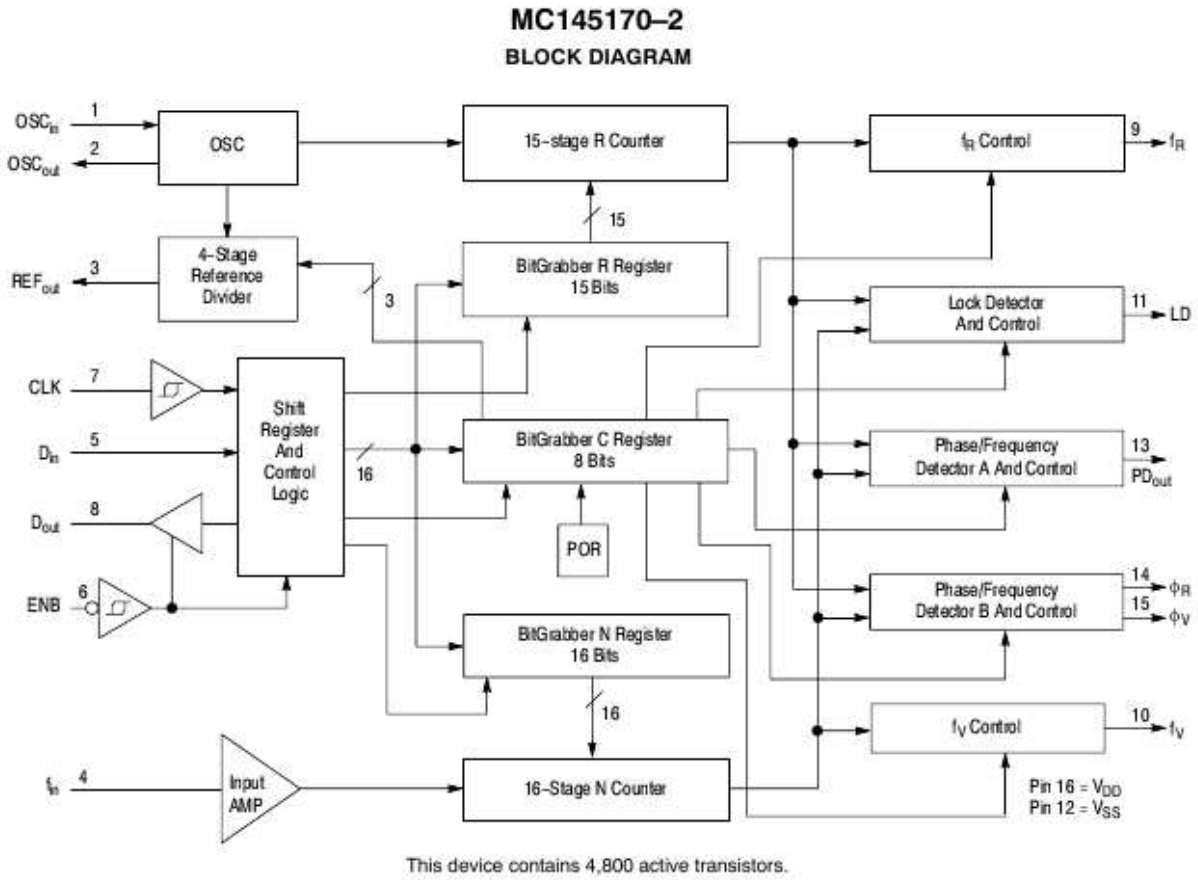
Phase Lock Loop and Voltage Controlled Oscillator

- Phase detector
- Prescalers to allow frequency tuning: $Frequency = (N/R)F_{CLOCK}$
- Thus F_{CLOCK}/R controls the frequency resolution.
- Loop filter to control the dynamic response
- Voltage controlled oscillator (VCO). For radiofrequency devices this is normally to be provided by the user as the quality output signal depend mostly on the VCO.

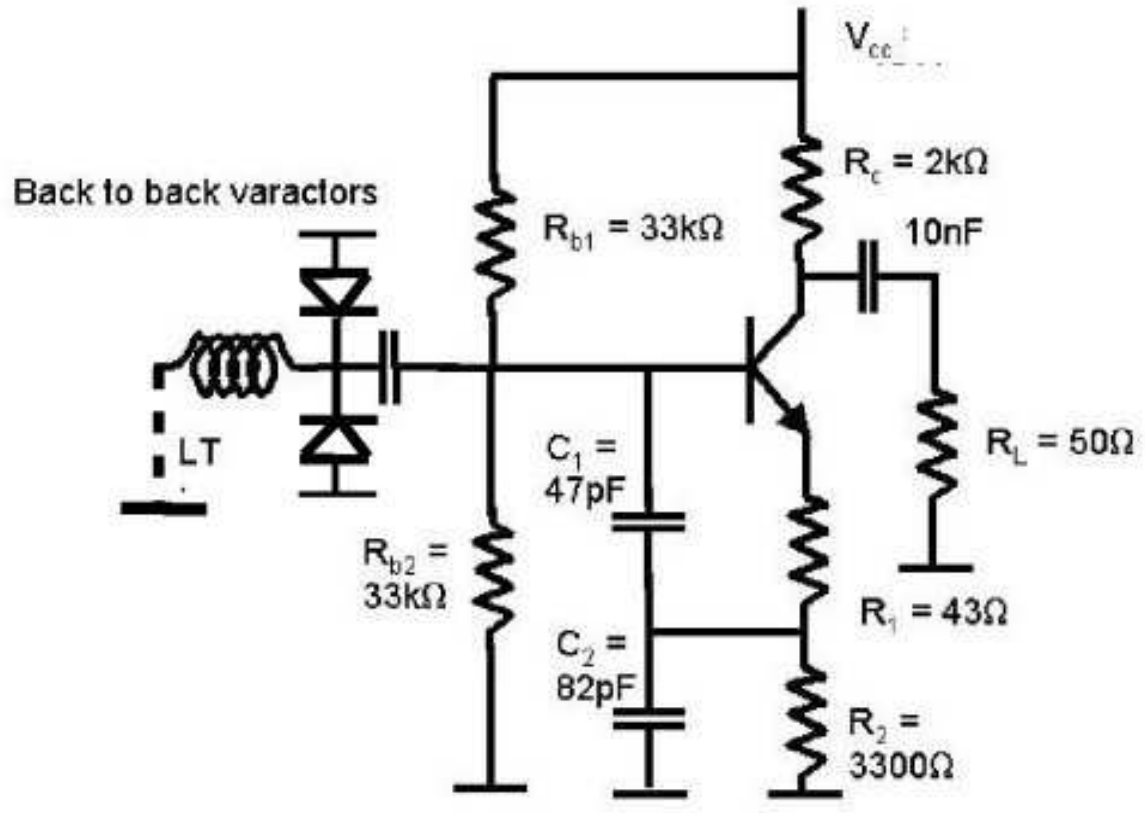
The MC145170

- Operates up to 185 MHz. But no internal VCO.
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Special patented bit grabbing interface to set the PLL parameters such as N and R prescaler values.

The MC145170

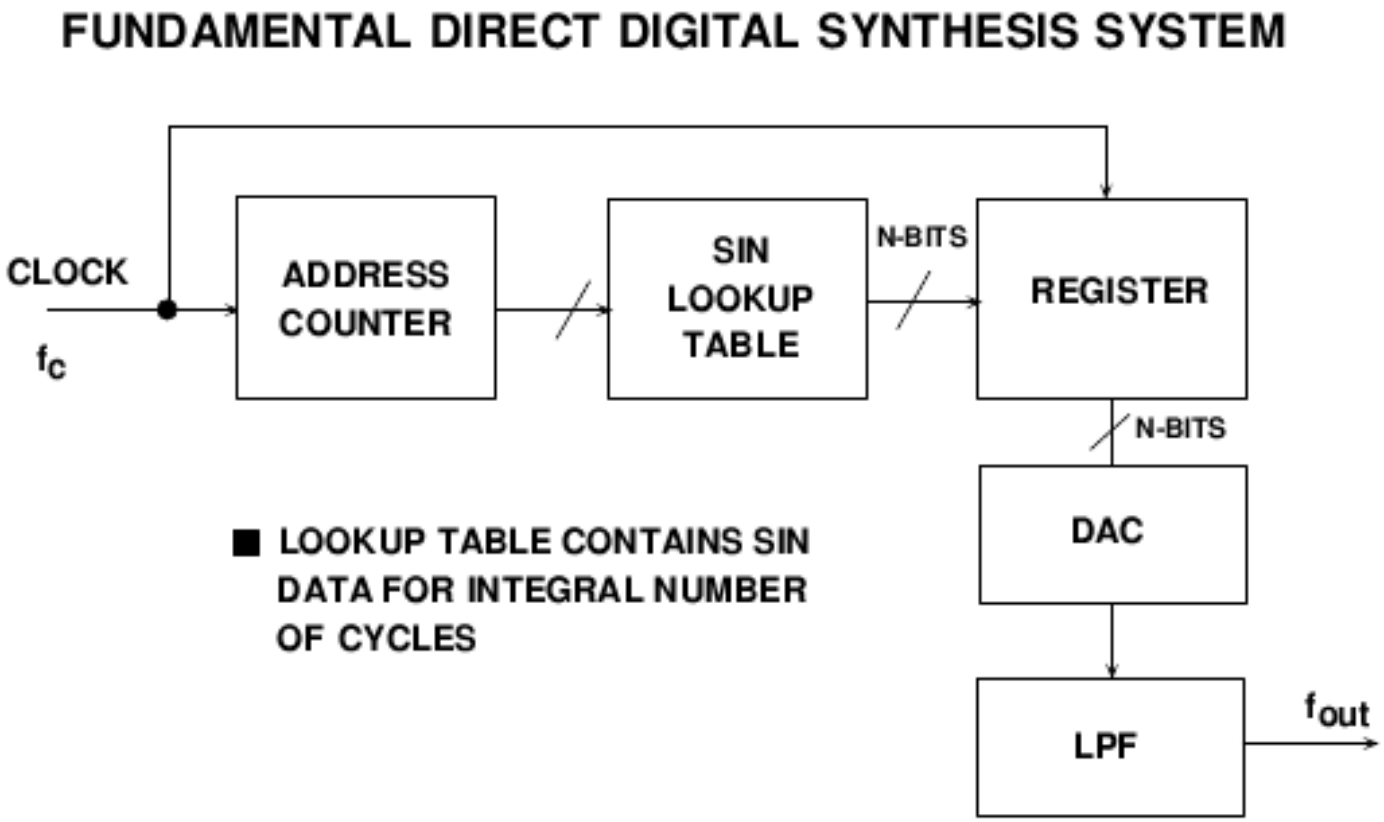


The Voltage Controlled Oscillator



The Direct Digital Synthesiser

- A totally digital device that produces a sine wave!



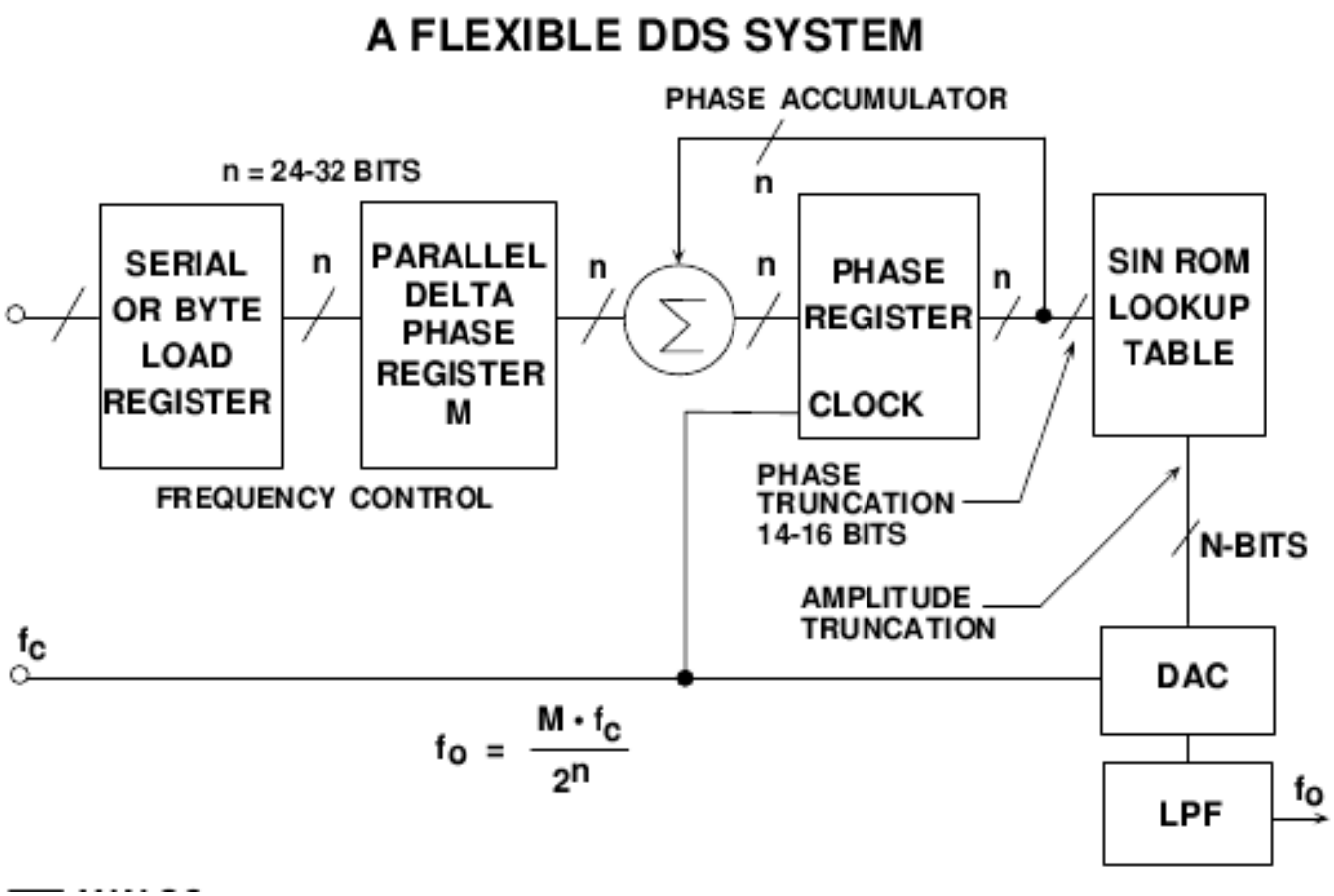
The Direct Digital Synthesiser

- An address counter fed by a clock cyclically reads out addresses into a sine wave **look up table**.
- The bytes in the L.U.T. represent a sine wave stored in memory.
- The L.U.T. is connected to a register that couples the L.U.T. address contents to a DAC, thus producing an anlogue sine wave.

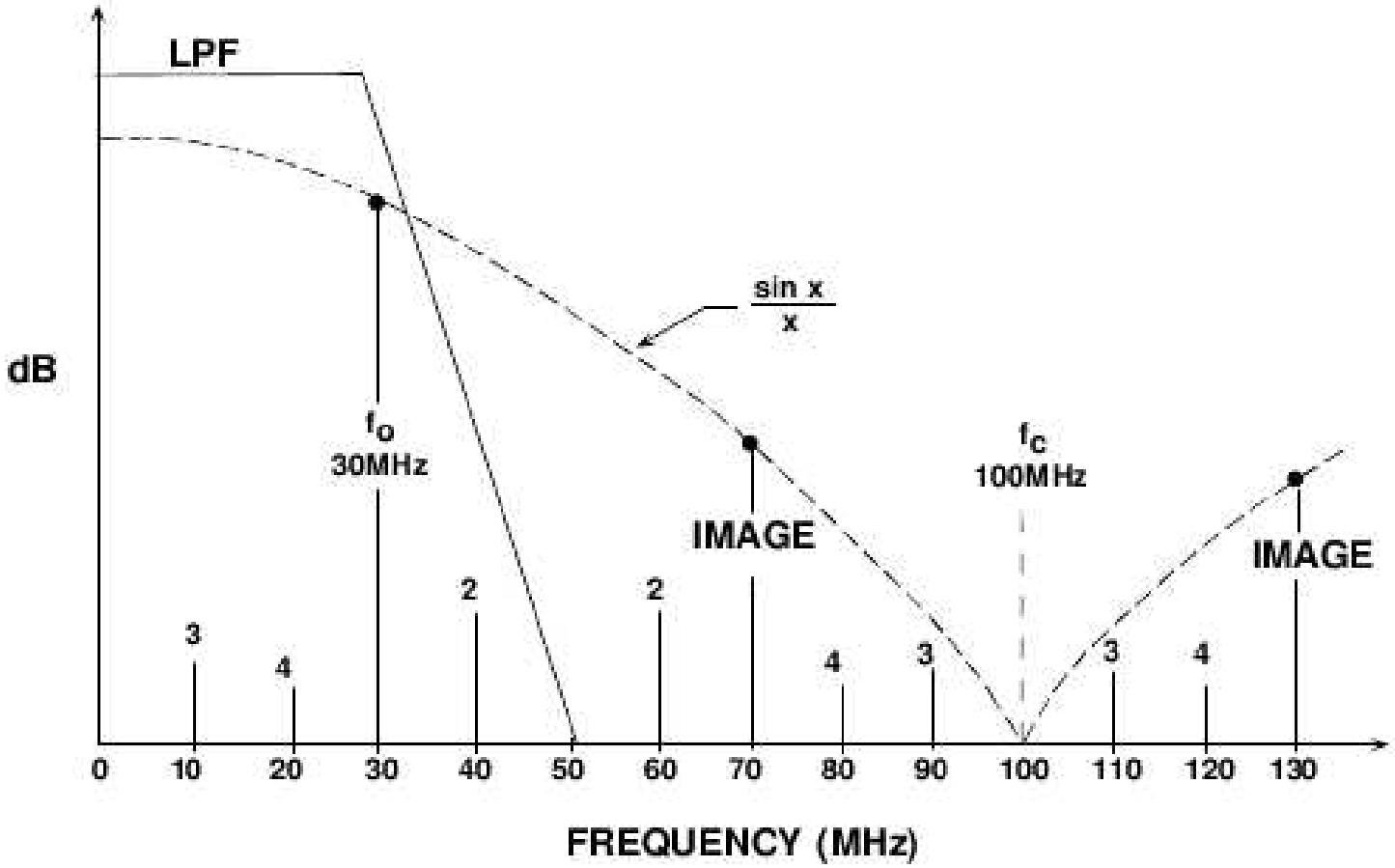
The Direct Digital Synthesiser

- A fundamental problem with this architecture is that the frequency cannot be varied except by changing the clock frequency.
- Consider a system in which the **delta phase or phase increment** is stored as well and added to **a phase accumulator**.
- This the **numerically controlled oscillator** hardware.
- The frequency at the output of the DDS is given by $f = (M f_{CLOCK})/2^M$.
- This gives a highly resolvable frequency.. 48 bits of resolution is common in the L.U.T.
- However the L.U.T. readout now occurs every M adress locations, and so the DDS is subject to **Nyquist's** theorem.
- Thus the highest frequency is half the clock frequency!

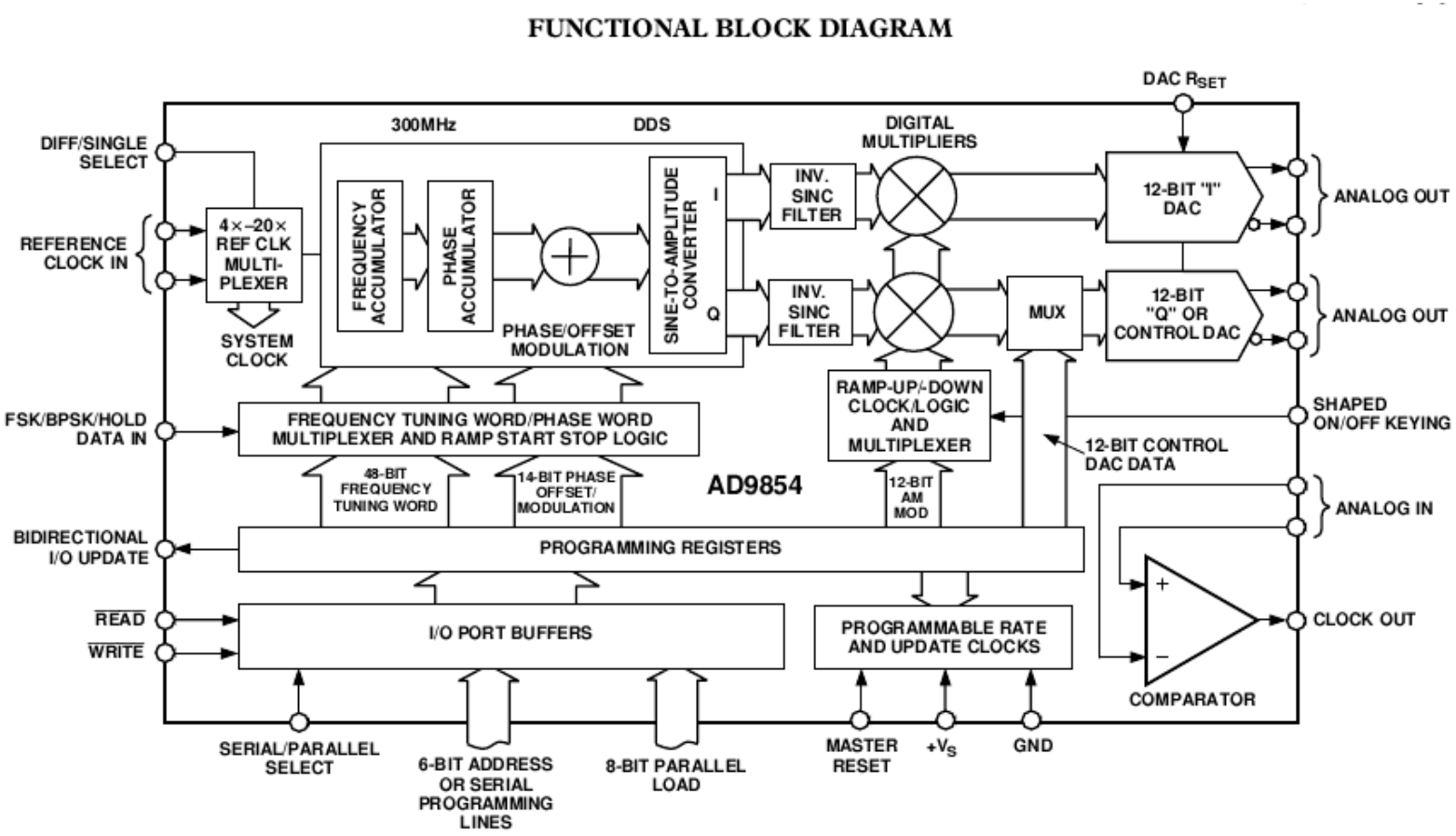
The Direct Digital Synthesiser



The Direct Digital Synthesiser



AD9854 Direct Digital Synthesiser



Perspective on Frequency Synthesisers

- PLL and VCOs are the way to produce up to microwave electromagnetic waves. This is because some form of tuning element is available to vary the frequency of the VCO which may work in the microwave range.
- For frequencies above about 10 GHz special semiconductor devices e.g. **Impatt sources** and **Gunn diodes** become available for low power applications. However these still need some frequency stabilisation.
- DDS and NCOs are complete digital solutions and are therefore restricted to frequencies.
- Often we need to embed a frequency synthesiser in digital hardware. In one limit this could be a sine wave generator in MATLAB when timing is non critical.
- For time critical applications wecan use a **Coordinate Rotating Digital Computer (CORDIC)**.

AD9874 IF Digitising Subsystem