Tri-level Bit-Stream Signal Processing Circuits and Applications

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Abstract— **We present signal processing building blocks for tri-level bit-stream signal processing (BSSP). These architectures are the 2-bit extensions from the existing 1-bit BSSP circuit modules. It is shown that the 2-bit designs offer better performance than their 1-bit counterparts. FPGA implementation results of both 1-bit and 2-bit designs are compared in terms of their hardware complexity. Finally, a digital phase locked loop (DPLL) and a quadrature phase-shift keying (QPSK) demodulator are presented as application examples of the proposed circuits.**

I. INTRODUCTION

Sigma-delta modulators (SDMs) are widely used for building analog-to-digital (A/D) and digital-to-analog (D/A) converters because of their simple circuitry and good tolerance against analog component accuracy [1]. Conventional digital signal processors (DSPs) operate at the Nyquist rate, and require the use of decimators and interpolators to interface to the over-sampled SDMs. With the development of bit-stream signal processing (BSSP) techniques [2-7], over-sampled bit-stream signals from the SDM output are processed directly, thereby eliminating the need for intermediate stages of decimators and interpolators. This leads to reduced hardware and circuit complexity. For example, a 40% reduction in logic gate count against multi-bit design is reported in a quadrature phase-shift keying (QPSK) demodulator design in [3].

Conventional BSSP circuits are targeted for 1-bit, 1st-order SDMs [2-6]. To improve the signal-to-noise performance, tri-level BSSP is investigated and two fundamental arithmetic circuits, namely, a tri-level bit-stream adder and multiplier are proposed in [8]. Based on the bit-stream adder and multiplier, other circuit modules in [2-4] can be extended to their ternary counterparts. More complex tri-level BSSP circuits and systems can be readily developed using these tri-level circuit modules as building blocks.

This paper presents the architectures of several tri-level BSSP circuit modules originating from the 1-bit designs in [2]. FPGA implementation results on circuit complexity and signal-to-noise performance are contrasted against conventional 1-bit realizations. Finally, to demonstrate the utility of the proposed tri-level BSSP circuit modules, a digital phase locked loop (DPLL) and a QPSK demodulator are realized and contrasted against the binary counterparts in terms of performance and circuit complexity.

II. TRI-LEVEL BIT-STREAM ARITHMETIC CIRCUTIS

We briefly review the tri-level bit-stream adder and multiplier. Details can be found in [8]. The output of the tri-level SDM is represented using 2's complement encoding, i.e., $-1 \to 11, 0 \to 00, 1 \to 01$.

A. Bit-Stream Adder

Fig. 1 shows the bit-stream adder. The circuit is described by the following z-domain equation

$$Z(z) = \frac{X(z) + Y(z) - (1 - z^{-1})LSB(z)}{2}. \quad (1)$$

To perform bit-stream subtraction, the subtractend is negated. The following logic equations can be shown to perform negation:

$$z_0 = x_0,$$
$$z_1 = \overline{x}_1 x_0. \quad (2)$$

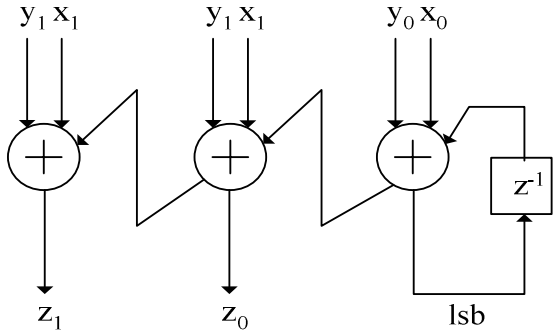

Figure 1. Tri-level bit-stream adder [8].

The average signal-to-noise-and-distortion ratio (SNDR) of the tri-level bit-stream adder is 9.0 dB higher than that of the bi-level adder.

B. Bit-Stream Multiplier

A tri-level bit-stream multiplier is depicted in Fig. 2. The circuit performs the multiplication of two bit-stream signals, $x[n]$ and $y[n]$ through the following operation:

$$z[n] = \frac{1}{L^2} \sum_{i,j=n-L+1}^{n} x[i]y[j], \tag{3}$$

where L is the time interval. The SNDR of the tri-level bit-stream multiplier has an average performance gain of 7.8 dB over the conventional bi-level design.

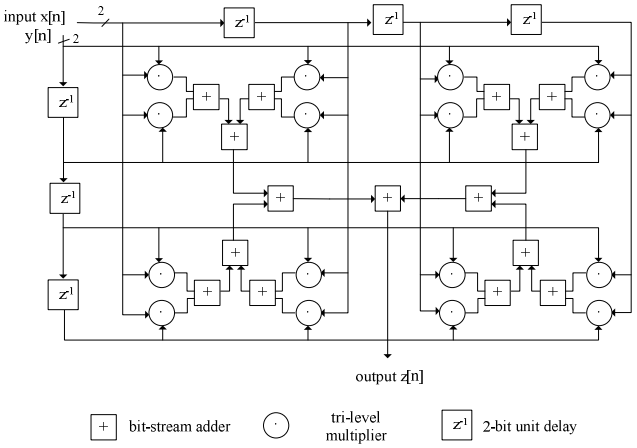

Figure 2. Tri-level bit-stream multiplier for $L = 4$ [8].

III. TRI-LEVEL BSSP CIRCUIT MODULES

In [2], five sigma-delta based circuit modules, namely, digital sigma-delta modulator (DSDM), bit-stream lowpass filter (LPF), bit-stream numerically controlled oscillator (NCO), bit-stream divider and bits-stream square root circuit (SQRT) are presented. The 2-bit extensions of these circuits are now explained. As the hardware complexity depends on the particular application, the FPGA implementation results on the resource utilization of both the propose tri-level architectures and the bi-level ones are presented in Section IV-B, in which a QPSK demodulator is implemented.

A. Digital Sigma-Delta Modulator (DSDM)

A DSDM is shown in Fig. 3. It converts the multi-bit input into tri-level bit-stream output. The feedback gain K defines the dynamic range of the multi-bit input, $x[n]$, which should be limited in the range $[-K, K]$ in order that the modulator works properly. The quantizer function $q(u)$ has the following characteristic:

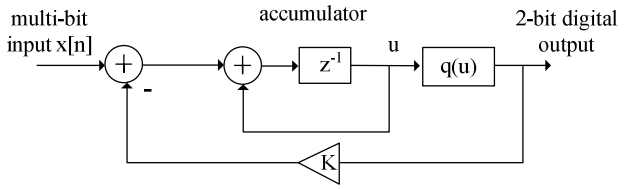

Figure 3. Digital sigma-delta modulator (DSDM).

$$q(u) = \begin{cases} -1, & u < -\alpha \\ 0, & -\alpha \le u \le \alpha \\ 1, & u > \alpha \end{cases}, \tag{4}$$

where α is the threshold. As explained in [8], the threshold is set to 0.25. This setup also simplifies the quantizer design. To demonstrate this, assume that K is set to 256, i.e., the bit-length of the input is 9 and that of the accumulator is 10. Then α is 64 and only the upper 4 bits are required to implement the quantizer as shown in Table I. Thus only two 4-input look-up tables (LUTs) are required in the FPGA implementation. If K is not a power of two, α can still be set as a power of two that is close to $0.25K$ because the effect of α to the signal-to-noise performance is not significant as discussed in [8].

TABLE I. QUANTIZER DESIGN

$u_{10}u_9u_8u_7$	q(u)
0001 … 0111	01
0000, 1111	00
1000 … 1110	11

B. Bit-Stream Lowpass Filter (LPF)

A first-order bit-stream LPF [7] is depicted in Fig. 4. Let $E(z)$ denotes the z-transform of the SDM noise, in the z-domain, it can be shown that the output $Y(z)$ and the state $W(z)$ (resp. the z-transforms of $y[n]$ and $w[n]$) are described by the following equations [2]:

$$W(z) = \frac{a}{1-(1-\frac{b}{K})z^{-1}} X(z) + \frac{-b}{1-(1-\frac{b}{K})z^{-1}} E(z). \tag{5}$$

$$Y(z) = \frac{\frac{a}{K}z^{-1}}{1-(1-\frac{b}{K})z^{-1}} X(z) + \frac{1-z^{-1}}{1-(1-\frac{b}{K})z^{-1}} E(z). \tag{6}$$

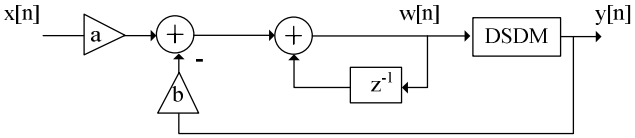

Figure 4. Bit-stream lowpass filter (LPF).

To demonstrate the performance gain of the tri-level bit-stream LPF over the bi-level counterpart, simulation of both tri-level and bi-level filters is carried out using the following parameters: $a = b = 6$, $K = 512$. The SNDR of the tri-level design is 62.5 dB while that of the bi-level LPF is 53.6 dB. The SNDR is determined by the ratio of the output power of a sinusoid, at a normalized frequency of 0.00189 (close to the cut-off frequency of the filter) and with a unity amplitude, to the total noise power in the frequency band of interest. The over-sampling ratio (OSR) is 128.

C. Bit-Stream Numerically Controlled Oscillator (NCO)

Fig. 5 shows a sigma-delta based oscillator. Compared with the original structure in [2], the proposed oscillator consists of two tri-level DSDMs with feedback gain K, two up/hold/down counters with upper and lower limits $\pm A$, $1 \ll A < K$ and circuit for the negation operation in (2). The up/hold/down counter increments, holds or decrements its count value when the tri-level input is 1, 0 or -1, respectively. The outputs of the oscillator ($Q_c[n]$ and $Q_s[n]$) are two sigma-delta modulated sinusoids that are $1/(2\pi K)$ in frequency, with a phase difference of $\pi/2$ between them.

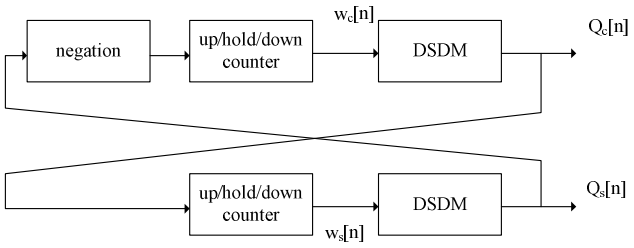

Figure 5. Sigma-delta based oscillator.

The frequency of the oscillator is controlled by the feedback gain K. If the gain K is changed by ΔK from the center value K_0 by a tri-level bit-stream control signal $c[n]$, the oscillator becomes an NCO. The oscillation phase $\theta[n]$ is [2]:

$$\theta[n] = \frac{n}{K_0} + \frac{\Delta K}{K_0^2}\sum_{i=0}^{n} c[i]. \qquad (7)$$

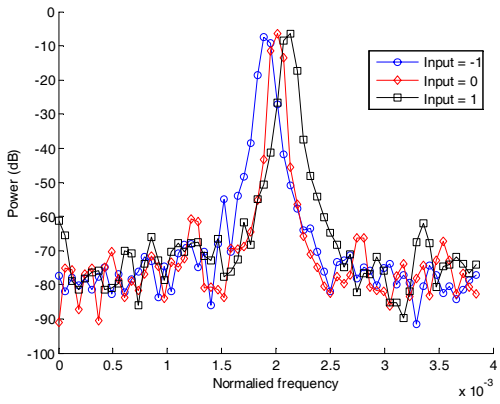

Figure 6. Power spectral densities of the bit-stream NCO.

To verify the operation of the NCO, Fig. 6 shows the power spectral density (PSD) plots of the output $Q_c[n]$ at three particular control inputs over the frequency band of interest. The simulation is carried out using the following parameters: $A = 75$, $K_0 = 79$, $\Delta K = 4$, OSR = 128. Using the same set of parameters, a tri-level bit-stream NCO and a bi-level counterpart are simulated to compare the signal-to-noise performance. The control input is set at 0. The SNDR of the tri-level NCO is 48.2 dB while that of the bi-level design is 42.2 dB.

D. Bit-Stream Divider

The block diagram of a bit-stream divider is shown in Fig. 7. The circuit implements the following nonlinear difference equation [2]:

$$z[n+1] = z[n] + \big(x[n] - y[n]z[n]\big)/(2K), \qquad (8)$$

where $x[n]$ and $y[n]$ are the inputs, $z[n]$ is the output and K is the feedback gain of the DSDM. Let $\overline{x}$ denotes the average value of $x[n]$. Similar to the original binary design, the average output $\overline{z}$ of the tri-level bit-stream divider converges to $\overline{x}/\overline{y}$. This is confirmed in the input/output characteristics plot depicted in Fig. 8. In the simulation, $\overline{x}$ is fixed at 0.037. A comparison of the average outputs from the tri-level design to that of the bi-level divider and the exact values is also shown in the same figure. It can be seen that both the tri-level and bi-level dividers converge closely to the exact value. Fig. 9 compares their output errors, where the output error is defined as the ratio of the difference of the exact value and the simulated output over the exact value. This verifies that the tri-level bi-stream divider achieves better performance than the bi-level counterpart.

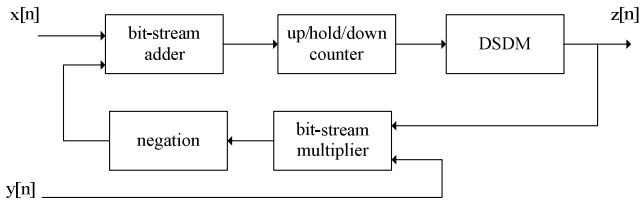

Figure 7. Bit-stream divider.

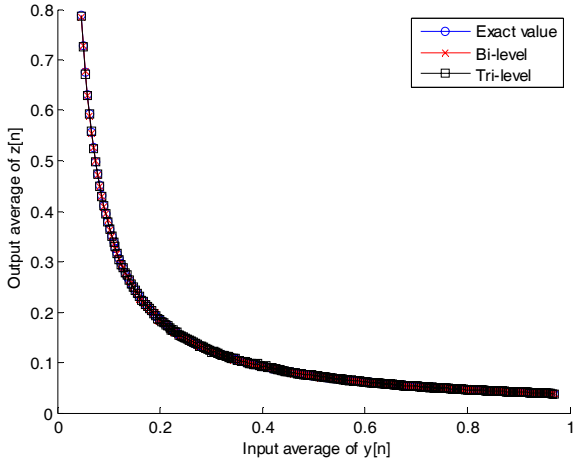

Figure 8. Input/output characteristics.

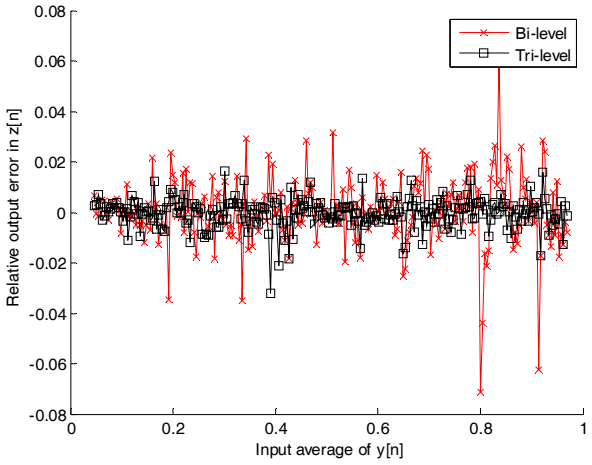

Figure 9. Output error plots of the tri-level and bi-level bit-stream dividers.

E. Bits-Stream Square Root Circuit (SQRT)

The architecture of the tri-level SQRT is shown in Fig. 10. The circuit implements the following difference equation [2]:

$$z[n+1] = z[n] + \left(x[n] - z[n]^2 \right) / (2K), \tag{9}$$

where $x[n]$ is the input, $z[n]$ is the output and K is the feedback gain of the DSDM. The average output $\overline{z}$ of the tri-level bit-stream divider converges to the square root of $\overline{x}$.

The input/output characteristics plots for the tri-level and bi-level designs are depicted in Fig. 11. Also shown in the figure is the exact value plot. Fig. 12 compares their output errors. Again, it can be seen that the tri-level SQRT achieves better performance than the bi-level SQRT.

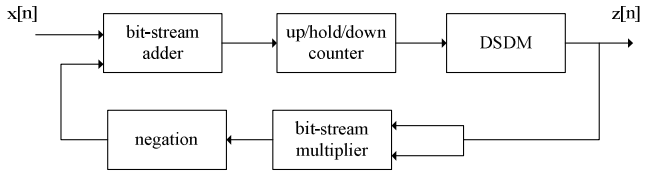

Figure 10. Bit-stream squart root circuit.

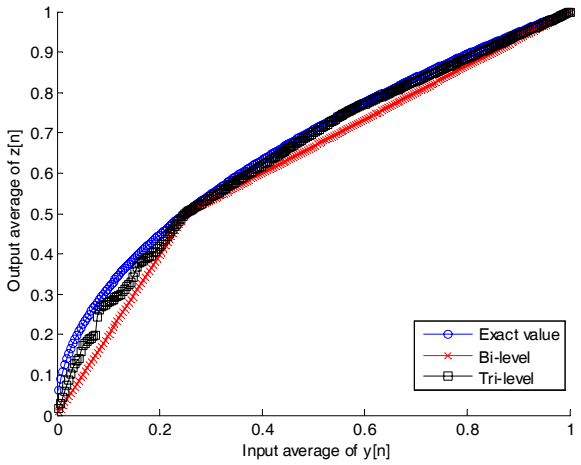

Figure 11. Input/output characteristics.

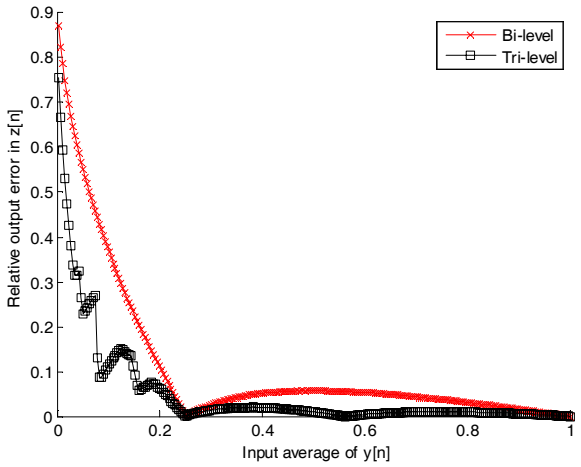

Figure 12. Output error plots of the tri-level and bi-level bit-stream dividers.

IV. Application Examples

In this section, two application examples, namely, a DPLL and a QPSK demodulator are described and the FPGA implementation results of the bi-level and tri-level designs are presented for comparison. The circuits are implemented with

the Xilinx Virtex-5 XC5VLX30 FPGA using the design tool ISE WebPACK 9.1i.

A. DPLL

A Type-1 DPLL [9] has been implemented with its block diagram shown in Fig. 13. The DPLL has a structure similar to the one presented in [4]. The input signal is assumed to be a complex sinusoid of the form

$$i[n] = i_c[n] + j \cdot i_s[n]. \tag{10}$$

The output of the bit-stream NCO is given by

$$q[n] = q_c[n] + j \cdot q_s[n]. \tag{11}$$

The phase detector is realized by two bit-stream multipliers and a bit-stream subtractor, and performs the following operation:

$$z[n] = \mathrm{Im}(i[n] \cdot q[n]^*), \tag{12}$$

where $\mathrm{Im}(x)$ denotes the imaginary part of x, and x^* denotes the conjugate of x. In this particular implementation, the normalized input frequency is 1/512. A, K_0 and ΔK are set to 80, 82 and 5, respectively. The OSR is 128. Simulations confirm that both bi-level and tri-level systems can synchronize to the input signal at steady state. The SNDRs of the bi-level and tri-level DPLL outputs are 35.5dB and 46.7dB, respectively. Table II shows the FPGA implementation results of the bi-level and tri-level DPLL designs. Comparison results with a multi-bit implementation can be found in [8].

TABLE II. IMPLEMENTATION RESULTS OF BI-LEVEL AND TRI-LEVEL DPLL DESIGNS

	Bi-level	Tri-level
No. of LUTs	122	208
No. of FFs	79	91

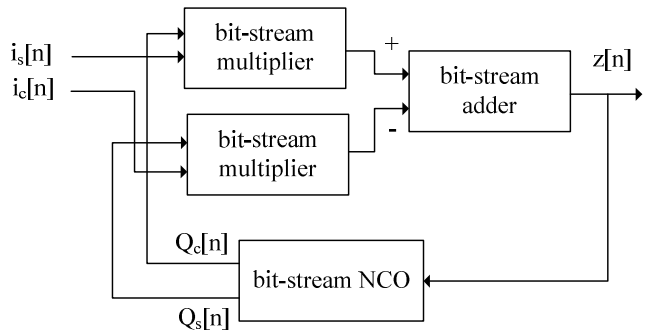

Figure 13. Type-1 DPLL.

B. QPSK Demodulator

The QPSK demodulator in [2] has been implemented using the proposed tri-level signal processing building blocks. The QPSK demodulator consists of the synchronization part shown in Fig. 14 and the phase detection part depicted in Fig. 15. The synchronization circuit implements the generalized Costas loop [10] and the phase detection part normalizes the output magnitude. The specification of this particular implementation for both the bi-level and tri-level designs is shown in Tables III & IV. Constellation plots of the output signals of the two designs are shown in Fig. 16. It can be seen that the tri-level design achieves more well-defined constellation which leads to a better performance. The FPGA implementation results of the bi-level and tri-level QPSK demodulators are shown in Table V. For a comparison on the hardware complexity of the tri-level and bi-level BSSP circuit modules, Table VI shows the FPGA resource utilization of individual component in this particular QPSK demodulator realization.

TABLE III. SPECIFICATION OF THE QPSK DEMODULATOR

Item	Specification
Input carrier	Sigma-delta modulated sinusodial wave with a normalized frequency of 0.002
Phase shift interval	5000
NCO parameter	$A = 75$, $K_0 = 79$, $\Delta K = 4$

TABLE IV. SPECIFICATION OF THE BIT-STREAM LPFS

Bit-stream LPF	Bi-level		Tri-level	
	Cut-off frequency	*Gain*	*Cut-off frequency*	*Gain*
(C)	$1.87\text{x}10^{-3}$	1.67	$1.87\text{x}10^{-3}$	1.33
(S)	$1.87\text{x}10^{-3}$	1.67	$1.87\text{x}10^{-3}$	1.33
(L)	$1.87\text{x}10^{-3}$	4	$1.87\text{x}10^{-3}$	16
(R)	$1.87\text{x}10^{-3}$	3	$1.87\text{x}10^{-3}$	3
(X)	$3.11\text{x}10^{-4}$	1	$3.11\text{x}10^{-4}$	1
(Y)	$3.11\text{x}10^{-4}$	1	$3.11\text{x}10^{-4}$	1

TABLE V. IMPLEMENTATION RESULTS OF BI-LEVEL AND TRI-LEVEL QPSK DEMODULATOR DESIGNS

	Bi-level	Tri-level
No. of LUTs	539	813
No. of FFs	380	419

TABLE VI. IMPLEMENTATION RESULTS OF BI-LEVEL AND TRI-LEVEL BSSP CIRCUIT MODULES FOR THE QPSK DEMODULATOR

Component	Bi-level		Tri-level	
	No. of FFs	*No. of LUTs*	*No. of FFs*	*No. of LUTs*
DSDM	11	11	11	13
LPF	21	31	21	33
NCO	36	61	36	86
Divider	41	53	47	86
SQRT	38	48	41	73

V. CONCLUSION

In this paper, we have presented various tri-level BSSP circuit modules which are the 2-bit extensions of the conventional 1-bit designs. In general, the tri-level implementations achieve better signal-to-noise performance than their bi-level counterparts at the expense of higher circuit complexity. To demonstrate the application of the proposed

tri-level BSSP building blocks, a DPLL and a QPSK demodulator have been implemented in FPGA and the hardware complexity of the tri-level designs has been contrasted with the conventional bi-level architectures.

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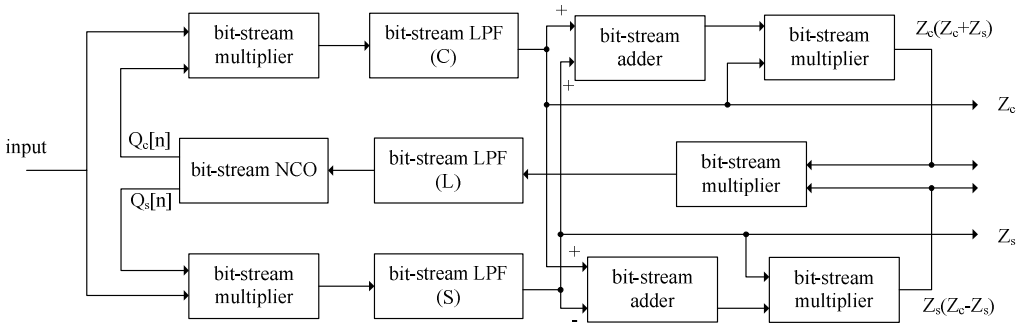


Figure 14. Synchronization part.

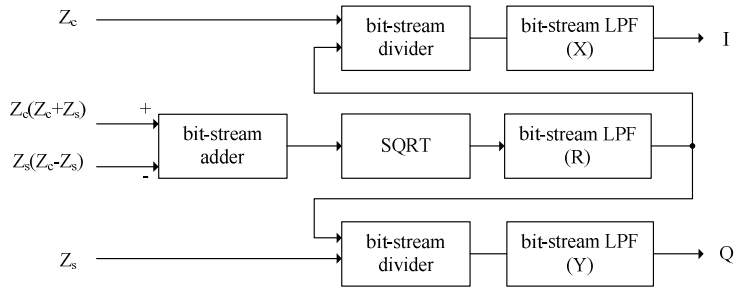
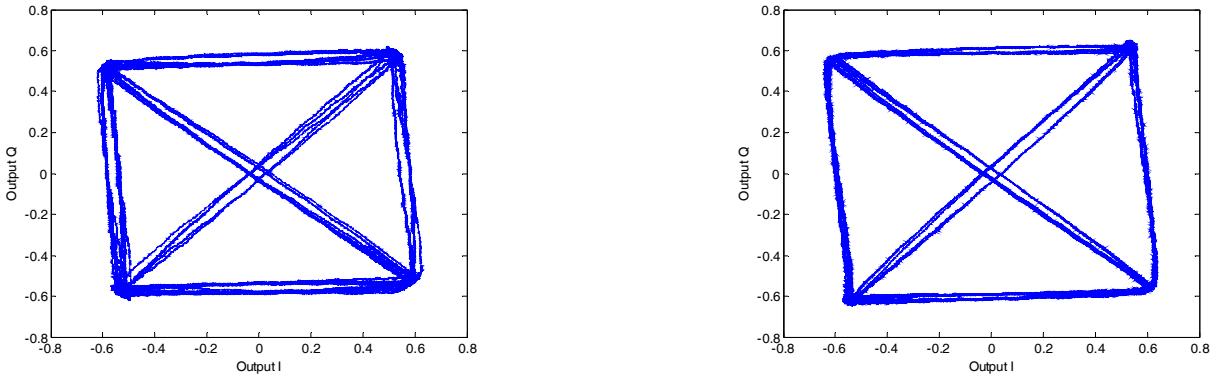


Figure 15. Detection part.



(a) (b)

Figure 16. Output constellation plots: a) bi-level design; b) tri-level design.