Implementation of UE Decoder for 3G LTE System at ETRI

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***Abstract*— In order to migrate toward 4G, studies on 3G LTE(Long Term Evolution) have been announced recently in the 3GPP(3rd Generation Partnership Project) and standardization is under way. Therefore, 3G LTE(Long Term Evolution) systems have been designed and developed over many countries. We also have been developing a 3G LTE testbed system at ETRI. 3G LTE system is adopting OFDM (Orthogonal Frequency Division Multiplexing) method, especially 2x2 MIMO (Multiple Input Multiple Output) OFDM and convolutional and turbo encoder for control channels and data channels respectively. In this paper, we describe the structure and implementation method of control channels and data channels of the UE decoder which is being developed at ETRI.**

Keywords-3G LTE; MIMO OFDM; Decoder;

I. INTRODUCTION

While current wireless systems can support majority of the emerging broadband services during the next several years, the need for a fundamentally new and efficient systems has been recognized. This has made several activities in standardization forums in recent years, like the work within 3G LTE study group. Wireless communication systems are evolving toward providing higher quality and higher speed multi-media services. In 3GPP, 3G LTE plan was established to overcome technical limits of 3rd generation mobile communication system in late 2004 and have a plan to finish writing Technical Report by June, 2006 and now standardization is under way to finish Technical Standard by June, 2007. MIMO(Multiple Input Multiple output) concept has been recognized as the key new technology to achieve required bandwidth efficiencies in 3G LTE and OFDM(orthogonal frequency division multiplexing) technique is the main physical layer design element for 3G-LTE downlink transmission scheme combined with either FDM (frequency division multiplexing) or TDM(time division multiplexing) as a multiple access method for the downlink shared data traffic channels.

In the field of wireless mobile communications, many companies and institutes are designing and developing 3G LTE systems over many countries and ETRI is one of them.

This paper is organized as follows. In the next section, we briefly introduce the 3G LTE testbed system which is being developed at ETRI, especially focused in the transport channel and control channel and data channel of UE decoder. In section 3, we introduce the structure and design method of UE decoder. In section 4, we analyzed the implementation result and computer simulation results of the viterbi decoder and the turbo decoder algorithm which are applied to this design. Finally, a summary of this article is given.

II. 3G LTE TESTBED SYSTEM

We are currently developing core technologies for a 3G LTE mobile communication system with high speed packet data transmission rates to take initiative on standardization and development of the 3G LTE testbed system. With related to these activities on standardization, ETRI is now developing the 3G LTE testbed. ETRI version of 3G LTE system is satisfactory to the specification of 3GPP.

Transport channels are composed of following 5 channels. PBCH(Primary Broadcast Channel) transmits information of system and timing of cell. DBCH(Dynamic Broadcast Channel) is used to broadcast variable SIB(System Information Block), its transport format is included in the control channel. PCH(Paging Channel) transmits Paging information. DL-SCH(Downlink Shared Channel) transmits some logical channels such as DCCH(Dedicated Control Channel) and DTCH(Dedicated Traffic Channel) and information of UL-SCH for random access is mapped to DL-SCH. MCH(Multicast Channel) transmits the p-to-m type signals for Multicast/Broadcast and logical channels of MTCH(Multicast Traffic Channel) for MBMS traffic and MCCH(Multicast Control Channel) for control information of MTCH are mapped to MCH.

L1/L2 Control information contains several types following information including downlink common control information, power control and feedback information for H-ARQ, etc.

Downlink Common Control Information(DL-CCI) means the information of resource allocation mode for DL-SCH, which contains the number of resource block, MIB(Master Information Block) change state.

Downlink Control Information(DL-CI) for PDSCH includes AMC, H-ARQ information, ACK/NACK channel information. This information is generated by BCCH RNTI in case of DBCH, by PAGING RNTI in case of PCH, by RA-RNTI in case of DL-SCH using Message-2 of Random Access

Procedure, by Temporary C-RNTI in case of DL-SCH using Message-4 of Random Access Procedure, by C-RNTI in case of other DL-SCH cases and transmitted by PDCCH(Physical Downlink Control Channel). DL-CI has two types of transport format(TF0, TF1), TF0 can have TYPE-1 and TF1 can have TYPE-1, TYPE-2.

Uplink Control Information(UL-CI) for PUSCH is control information of response for uplink data channel request, includes resource allocation, AMC, H-ARQ information. This is generated by using RA-RNTI in case of UL-SCH (Message-3) and by using C-RNTI in case of other DL-SCH cases and is transmitted by PDCCH. UL-CI can have one type of transport format(TF0 TYPE-0).

ACK/NACK Information for UL-SCH is defined to each UE, and is transmitted by PFBCH. One subframe can use upto N^{FB}_{max} (= 50 for 10MHz BW, 100 for 20MHz BW).

Transmit Power Control Information for Uplink is defined to each UE, and is transmitted by PTPCH. One subframe can use upto N^{TPC}_{max} (= 16 for 10MHz BW, 32 for 20MHz BW).

Mapping to physical channels and physical signals are as follows.

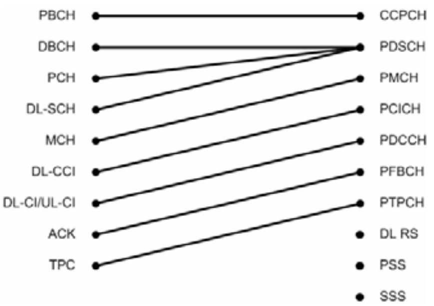

Figure 1. Mapping to physical channels and physical signals

III. 3G LTE UE DECODER

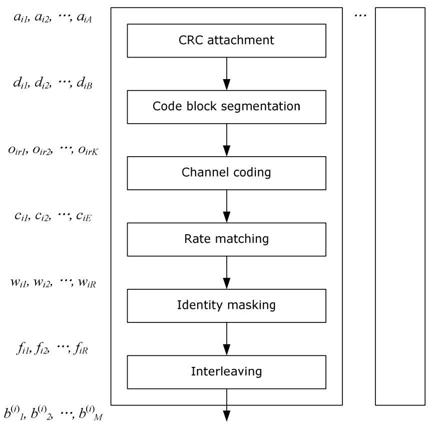

Figure 2. Multiplexing and coding mechanism

Convolutional code with code rate = 1/3 has following polynomials

G_0 = 557 (octal), G_0 = 663 (octal), G_0 = 711 (octal)

Function of the Turbo Encoder is described in fig.2 . Transfer function of this encoding is

$$G(D)=\left[1, \frac{g_1(D)}{g_0(D)}\right]$$, where $g_0(D) = 1 + D^2 + D^3$ and $g_1(D) = 1 + D + D^3$.

Encoded signals output with the order $x_1, z_1, z'_1, x_2, z_2, z'_2, \ldots, x_K, z_K, z'_K$. Whereas, in case of Trellis termination, next order is applied. $x_{K+1}, z_{K+1}, x_{K+2}, z_{K+2}, x_{K+3}, z_{K+3}, x'_{K+1}, z'_{K+1}, x'_{K+2}, z'_{K+2}, x'_{K+3}, z'_{K+3}$

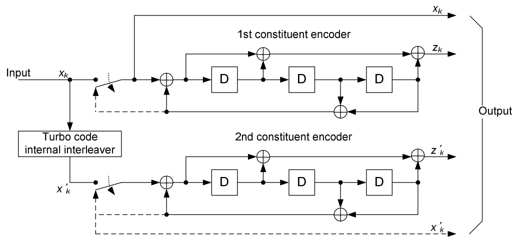

Figure 3. Turbo encoder with rate=1/3 and state=8 (dotted line only for trellis termination)

Hybrid ARQ(Automatic Repeat ReQuest) algorithm is performed with 8 channels. Chase combining method and various types of IR(Incremental Redundancy) techniques are applied. Figure below shows the algorithm of Hybrid ARQ rate matching operation.

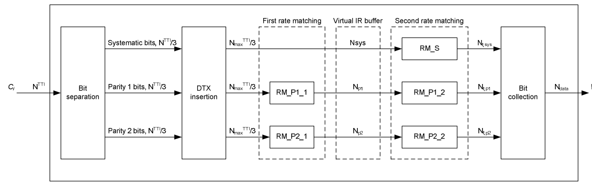

Figure 4. H-ARQ rate matching functionality

In downlink, De-Rate Matching Algorithms for PDSCH0 & PDSCH1 are constructed with two stages. First stage is dependent of IR buffer size and second stage rate matching is relevant to the physical block size.

Following figure means the decoding procedure of each control channel and data channels.

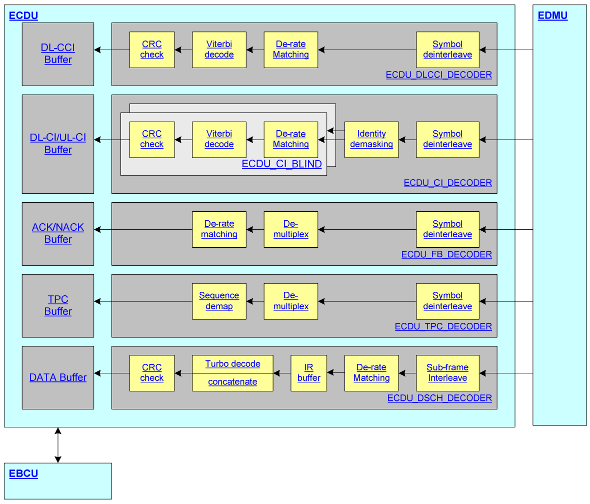

Figure 5. Procedure of UE Decoder

ECDU_CCI_DECODER operates decoding procedure by the reverse order of PCICH encoding. Input signals can have two size of data according to the transmission bandwidth. 20MHz bandwidth has 288 LLR input, whereas 10MHz transmission case has 200 LLR input data. DL-CCI can basically have four types of fixed period(1, 2, 5, 10ms).

ECDU_CI_DECODER decodes maximum 32(or 16) PDCCH units from EDMU. In this decoded data, transport channel ID, control type, resource block assign information, assign duration, modulation order, transport block size, RV(redundancy version) parameters, new data indicator, ACK, H-ARQ ID information are contained.

Deinterleaving is performed by the PDCCH unit, column-by-column to 25x6 size, next is inter-column permutation. Next stage is identity de-masking, which uses encoded 72 data allocated 16 bit RNTI. With this sequence, de-masking algorithm is done. Afterthat, de-rate matching is performed by the 150 LLR PDCCH unit. PDCCH is detected by blind detection with the successive two PDCCH units. Detected types are as follows.

TF0 with first PDCCH unit, TF0 with second PDCCH unit, TF0 with first and second PDCCH units, TF1 with first and second PDCCH units

ECDU_FB_DECODER receives maximum 32 PFBCH LLR from demodulator and accumulates the received data.

ECDU_TPC_DECODER detects TPC 3bits by sequence mapping after receiving 12 PTPCH LLR from demodulator. In the TPC information, MSB 1bit is repeated 6 times, next MSB 1bit is repeated 4 times, LSB 1bit is repeated twice.

ECDU_DSCH_DECODER performs decoding operation of PDSCH LLR from demodulator using DL-CI information. Serial method for multiple codeword is applied to use MMSE-SIC. De-rate matching algorithm is as follows.

if puncturing is performed
    $e = e_{ini}$
    $m = 1$
    do while $m \le X$
        $e = e - e_{minus}$
        if $e \le 0$
        set bit x_m *to* δ *where* $\delta \notin \{0, 1\}$
        $e = e + e_{plus}$
        end if
        $m = m+1$
    end do
else repetition is performed
    $e = e_{ini}$
    $m = 1$
    do while $m \le X$
        $e = e - e_{minus}$
        do while $e \le 0$
        repeat bit x_m
        $e = e + e_{plus}$
        end if
        $m = m+1$
    end do
end if

Turbo decoder implemented in this system is using consecutive 3 memory convolutional encoders, MAP decoder is applied to each convlutional encoder. Fig.xx shows the structure of turbo decoder, 2 MAP decoder decodes each convolutional encoder. Turbo decoding starts from MAP decoder 1 and ouputs the result to MAP decoder 2. MAP decoder 2 operates MAP decoding with the information of channel and MAP decoder 1. Repeatedly, output of MAP decoder 2 is input to MAP decoder 1. As there are an interleaver and a deinterleaver before and after MAP decoder of 2nd consitituent code, each output of MAP decoder should be the LLR of systematic bit of the same position.

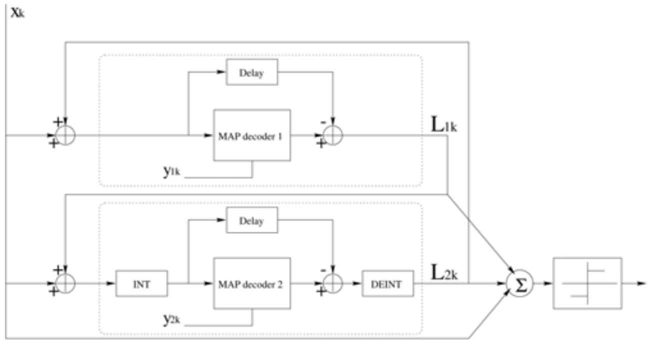

Figure 6. Conceptual block diagram of Turbo decoder

CRC uses 24 CRC parity as

$$g_{CRC24}(D) = D^{24} + D^{23} + D^{6} + D^{5} + D + 1$$

IV. IMPLEMENTATION RESULT

TABLE I. SIMULATION PARAMETERS

	PHY Implementation Spec.
Multiple Access/Duplex	OFDM (OFDMA)/ FDD,FH
Channel Codec	Convolutional, Turbo coding
Modulation Level	QPSK, 16-QAM, 64-QAM

UE decoder of 3G LTE testbed system at ETRI is composed of two FPGA(Field Programmable Gate Array) units, first one, ECDU1, contains the functions of control channel decoding and Hybrid ARQ and Channel De-rate matching, and another one, ECDU2, is fully implemented with turbo decoder that can cover 2x2 MIMO channels.

We implemented UE decoder with Xilinx Virtex2pro VP100 FPGA. As a result of the implementation, ECDU1 FPGA uses 85%(37481/44096) of slice and 95%(422/444) of block memory and ECDU2 FPGA uses 95%(41891/44096) of slice and 100%(444/444) of block memory.

Figures below depict the real implementation UE system and two FPGA UE decoder units of 3G LTE testbed system at ETRI.

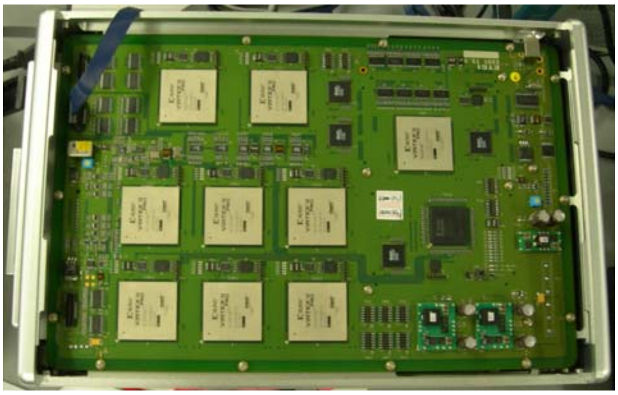

Figure 7. UE testbed system of 3G LTE at ETRI

Figure 8. FPGA UE decoder units of 3G LTE at ETRI

Simulation Results

We compared the fixed point simulation result with floating point simulation result of viterbi decoder and trubo decoder and verified that these results are satisfactory with the system requeirement of specification.

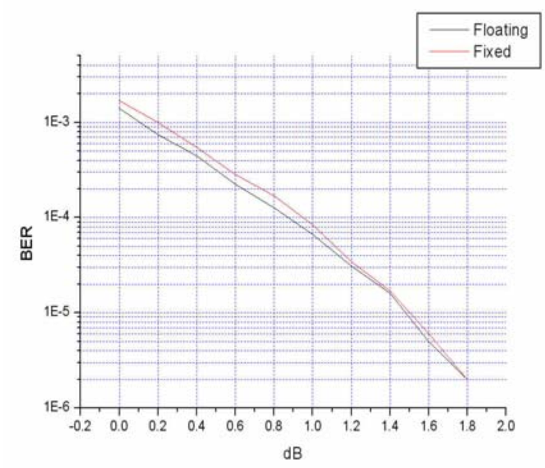

Figure 9. BER of Viterbi Decoder

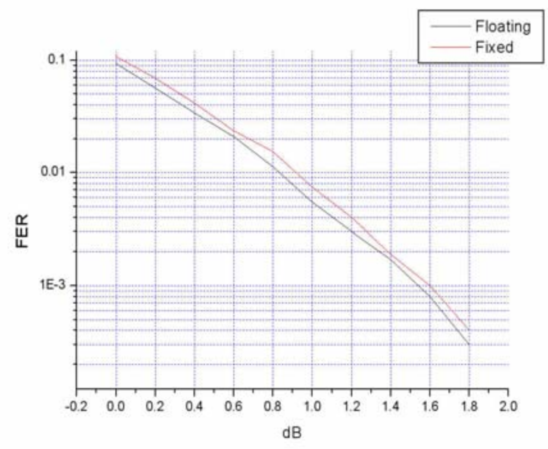

Figure 10. FER of Viterbi Decoder

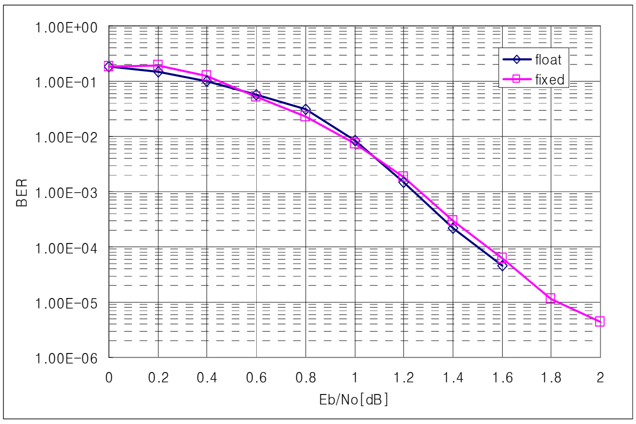

Figure 11. BER of Turbo Decoder

V. CONCLUSIONS

In this paper, we showed how to design the algorithm and structure of the implemented UE decoder for 3G LTE testbed system at ETRI. Especially, we focused on the part of control information structure and de-rate matching algorithm. Finally, we showed the performance of the viterbi decoder and turbo decoder which are implemented in this system. It is verified that the implemented performance of this UE decoder satisfies the requirement of the 3G LTE system.

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