# Optimal Detection of IDMA Signals


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***Abstract*— In this paper the system model of an uncoded and fully synchronised interleave division multiple access (IDMA) scheme is transformed into an equivalent matrix model. This new model allows for additional alternative insights into the principles of IDMA and it is shown that the arising matrices are highly structured and very sparse. Furthermore the optimal detector for IDMA is derived and compared to the standard iterative decoder. We use EXIT charts and an empirical rank analysis to highlight that systems without an alternating signature mask always have a low rank and that parallel interference cancellation then fails.**


## I. Introduction

Among the various communication techniques that have been studied, direct sequence code division multiple access (DS-CDMA) systems have grown popular and extensively studied. The basic idea is to assign each user a unique code sequence that is applied to each bit and allows for a separation at the receiver side of the communications link. The process of applying the code sequence is usually referred to as spreading a bit into several chips, and traditionally the data stream of each user is interleaved prior to spreading with the aim of distributing consecutive bits over a longer period of time. Motivated by this principle the order of spreading and interleaving can also be swapped resulting in a chip interleaved system rather than a bit interleaved system. Sometimes this technique is referred to as chip-interleaving [1] and sometimes as interleave division multiple access (IDMA) [2, 3].

In [2] the details of IDMA were described, and motivated by soft interference cancellation techniques and iterative turbo decoding schemes, an iterative receiver was proposed. Equipped with this low complexity yet very powerful receiver it was shown by simulation and density analysis [4–6] that the performance of such systems is close to the achievable maximum. In [7, 8] power allocation schemes for IDMA were investigated and in [3] it was shown that the capacity of IDMA systems for Gaussian channels is only limited by noise. Work on how to efficiently generate and distribute interleaver configurations throughout the network was carried out in [9].

Clearly, numerous aspects of IDMA have been extensively studied but the transmitter side has had little investigation so far. In this paper we show that the system model of every IDMA system can be converted into a matrix representation that allows for a much greater insight into the IDMA principal. Based on this model the optimal detector is derived and for reasonably small systems the performance is compared to the iterative receiver proposed in [2].

At the core of any IDMA system is a chip interleaver and a repetition encoder[2]. Using parallel interference cancellation (PIC) a repetition encoder that does not only repeat the bit but also alternates its sign as used in [2, 4, 5] is needed to prevent catastrophic performance.

This process will be referred to as *masking* and for the alternating pattern we will coin the term “flip-mask”. With an empirical analysis of the matrix model we show that such systems are usually severely rank deficient whereas using a flip-mask will provide matrices that are rank deficient by at most one.

In this paper vectors are $\mathbf{x} = (x_1, \ldots, x_n)$, whereas $\mathbf{x}_1$ and $\mathbf{x}_2$ denote two different vectors but the elements of such vectors are never addressed explicitly. Random variables/vectors are denoted by capital letters only. To address the $k^{\text{th}}$ column of the matrix $\mathsf{G}$ we write $\mathsf{G}(\cdot, k)$, and to address just a single element we write $\mathsf{G}_{i,j}$. The bit energy is always 1 and the signal to noise ratio in this paper is defined as

$$\text{SNR} \triangleq \frac{1}{\sigma^2},$$

where $\sigma^2$ is the noise power.

The paper is organised as follows: in Section II the matrix model is derived and some basic matrix properties including the sparseness are investigated. Section III is dedicated to deriving the optimal detector for IDMA, Section IV shows performance analysis using BER and EXIT charts and Section V empirically deals with the masking issue of IDMA and identifies a link between the matrix rank and the system performance.

## II. Alternative Transmitter Model

As in [2] the usual transmitter structure for an IDMA system with $n$ users is depicted in figure 1. Each user $k$ has a designated bit vector $\mathbf{B}_k$ to transmit, a rate $r$ repetition encoder (spreader) that maps the bit vector $\mathbf{B}_k$ to the chip vector $\mathbf{X}_k$ and finally a chip interleaver $\varphi_k$ that is different for each user and usually picked at random. The sent data vector $\mathbf{Z}$ is then


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[2]The term *spreading* and *repetition encoding* are interchangeable, and hence the code rate $r$ is the inverse of the spreading gain

the sum of all interleaved chip-streams and the transmitter side of the system is modelled as [2, 4, 5, 8, 9]

$$Z_j = \sum_{k=1}^{n} Y_k. \tag{1}$$

This system model essentially starts at the interleaved chip level (dashed box in figure 1) and has two major shortcomings:

1) the actual mask- and interleaver choice does not show up and consequently there is no way to optimise them based on this model
2) it *assumes* that the transmitted signal $\mathbf{Z}$ is decomposable into the data streams $\mathbf{B}_1$ to $\mathbf{B}_n$ and it is easy to construct cases where this is not true

To elaborate on point 2, simply consider the case where all interleavers are identical and all users use the same mask (e.g. flip-mask), then there is no parameter left that uniquely identifies the users.

The model we are going to propose now does not bear these shortcomings and accurately models the IDMA signal $\mathbf{Z}$ based on the user data, interleaver and mask selection, and will turn out as

$$\mathbf{Z} = \mathsf{G}\mathbf{B}, \tag{2}$$

where $\mathbf{B}$ is the user data and $\mathsf{G}$ describes the chosen interleaver and mask. Contrary to the traditional model (1), our system model also allows for a better mathematical insight into the fundamental IDMA principle.

We are now going to show how $\mathsf{G}$ and $\mathbf{B}$ relate to the data streams $\mathbf{B}_k$ and used interleavers $\varphi_k$ and masks.

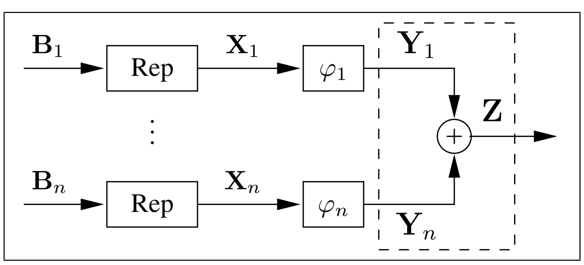



Fig. 1. Transmitter part of IDMA system for $n$ users

The repetition encoding of the data stream $\mathbf{B}_k$ is described by

$$\mathbf{X}_k = \begin{bmatrix} \mathbf{1} & 0 & 0 \\ 0 & \ddots & 0 \\ 0 & 0 & \mathbf{1} \end{bmatrix} \mathbf{B}_k = \mathsf{G}_k \mathbf{B}_k,$$

where $\mathbf{1}$ denotes the all ones column vector of length $1/r$ to achieve a rate $r$ repetition encoding and $\mathsf{G}_k$ denotes the generator matrix. Interleaving the chip stream $\mathbf{X}_k$ is equivalent to permuting the corresponding rows in the generator matrix $\mathsf{G}_k$ (note that $\mathsf{G}_k$ is usually not square). Let $\mathsf{G}'_k$ denote the result of permuting the rows of $\mathsf{G}_k$ according to the interleaver $\varphi_k$, then the encoding and interleaving operation for user $k$ is fully described by

$$\mathbf{Y}_k = \mathsf{G}'_k \mathbf{B}_k,$$

and the output signal can be written as

$$\mathbf{Z} = \sum_{k=1}^{n} \mathbf{Y}_k = \sum_{k=1}^{n} \mathsf{G}'_k \mathbf{B}_k = \begin{bmatrix} \mathsf{G}'_1 & \dots & \mathsf{G}'_n \end{bmatrix} \begin{bmatrix} \mathbf{B}_k \\ \vdots \\ \mathbf{B}_n \end{bmatrix}.$$

Introducing the formal substitutions

$$\mathsf{G} \triangleq [\mathsf{G}'_1 \dots \mathsf{G}'_n] \tag{3}$$
$$\mathbf{B} \triangleq [\mathbf{B}_1 \dots \mathbf{B}_n]^T, \tag{4}$$

the fully synchronised IDMA transmitter can be described in the compact form

### A. Example for 2 Users, r=1/2, Interleaving over 4 Chips

Let the two users be denoted $\mathscr{A}$ and $\mathscr{B}$ transmitting the bit vectors $\mathbf{A} = (A_1, A_2)$ and $\mathbf{B} = (B_1, B_2)$ and using the interleaver mappings $\varphi_A$ and $\varphi_B$ respectively, the process is illustrated as follows:

$$\mathscr{A} : (A_1, A_2) \xrightarrow{\text{Rep.}} (A_1, A_1, A_2, A_2) \xrightarrow{\varphi_A} (A_1, A_1, A_2, A_2)$$
$$\mathscr{B} : (B_1, B_2) \xrightarrow{\text{Rep.}} (B_1, B_1, B_2, B_2) \xrightarrow{\varphi_B} (B_1, B_2, B_2, B_1).$$

In this case the interleaver for user $\varphi_A$ does not alter the chip stream at all, and $\varphi_B$ exchanges the second and the fourth chip. The transmitted signal vector $\mathbf{Z}$ is the sum of the two interleaved chip vectors. The same process can be elegantly expressed with matrices as will be shown now.

Both users use the same spreading code so the respective generator matrices are

$$\mathsf{G}_A = \mathsf{G}_B = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix}.$$

Swapping the rows in $\mathsf{G}_A$ and $\mathsf{G}_B$ according to the interleavers $\varphi_A$ and $\varphi_B$ yields

$$\mathsf{G}'_A = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \qquad \mathsf{G}'_B = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}.$$

The final system matrix is then

$$\mathsf{G} = [\mathsf{G}'_A \quad \mathsf{G}'_B] = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix},$$

and the interleaved chip stream is obtained by

$$\mathbf{Z} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} A_1 + B_1 \\ A_1 + B_2 \\ A_2 + B_2 \\ A_2 + B_1 \end{bmatrix}$$

### B. Matrix Properties

Let $l_b$ denote the block length of the encoder, then IDMA systems are using an $(l_b/r, l_b)$ repetition code. Consequently the dimension of the generator matrix for every user $k$ is

$$\dim(\mathsf{G}_k) = \frac{l_b}{r} \times l_b.$$

Because the chip interleaver only permutes the columns of $\mathsf{G}_k$,

$$\dim(\mathsf{G}'_k) = \dim(\mathsf{G}_k).$$

With the definition of the system matrix in (3) its dimension is

$$\dim(\mathsf{G}) = \frac{l_b}{r} \times n l_b.$$

For fully loaded systems the code rate is $r = 1/n$ and $\mathsf{G}$ becomes a square matrix, i.e. there is one equation for each bit.

The system matrix $\mathsf{G}$ is very structured and contains only elements from the set $\{0, +1\}$. From the repetition encoding it holds that each column contains exactly $1/r$ non-zero entries. Furthermore each row of $\mathsf{G}_k$ (and also $\mathsf{G}'_k$) contains one non-zero entry, and as $\mathsf{G}$ is composed of $n$ such matrices, the number of nonzero entries is exactly $n$, or more formally

$$\sum_{k=1}^{l_b/r} |\mathsf{G}_{k,j}| = 1/r, \qquad 1 \leq j \leq n l_b \tag{5}$$

$$\sum_{k=1}^{n l_b} |\mathsf{G}_{j,k}| = n, \qquad 1 \leq j \leq l_b/r. \tag{6}$$

For fully loaded systems each row and column sums to $n$ and using (6) the number of non-zero elements computes to $n l_b/r$. As a measure of sparseness, the ratio $s$ of the number of nonzero elements over the total number of elements of $\mathsf{G}$ is introduced and turns out as

$$s = \frac{\frac{n l_b}{r}}{\frac{l_b}{r} n l_b} = \frac{1}{l_b}, \tag{7}$$

and depends neither on the code rate $r$ nor the number of users $n$ anymore but is a function of the block length $l_b$ only. In [5] for instance a block length of $l_b = 128$ is used which translates to $s = 1/128$ or less than 1% of non-zero values.

## III. Optimal Detector

Figure 2 shows the extension of the system model (2) by a (possibly stochastic) channel model $\mathsf{H}$ and additional noise $\mathbf{N}$. The received signal vector $\mathbf{R}$ is obtained by

$$\mathbf{R} = \mathsf{HG}\mathbf{B} + \mathbf{N}. \tag{8}$$

For the derivation of the optimal detector the channel matrix $\mathsf{H}$ is assumed to be deterministic and the noise model is additive white Gaussian noise (AWGN). For simplicity of notation the auxiliary matrix

$$\mathsf{M} \triangleq \mathsf{HG}$$

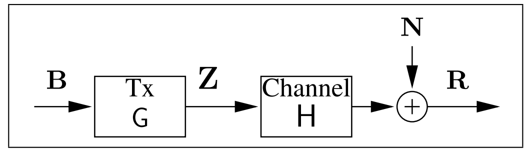



Fig. 2. Generalised IDMA model including a channel and noise

is introduced. The system model is then summarised as

$$\begin{aligned} &\mathbf{R} = \mathsf{M}\mathbf{B} + \sigma\mathbf{N} \\ &\mathbf{B} \in \mathcal{B}, \qquad \mathsf{M} \in \mathbb{R}^{n\times n} \\ &N_k \sim \mathcal{N}(0,1) \quad \text{and i.i.d.} \quad \forall k \\ &B_k \sim \mathcal{U} \quad \text{and i.i.d.} \quad \forall k \end{aligned}$$

where $\mathcal{B}$ denotes the set of source symbol vectors, $\mathcal{N}(0,1)$ a zero mean Gaussian random variable with power 1 and $\mathcal{U}$ a uniform distribution. Consequently, for a given data vector $\mathbf{b}$, $R_k$ is a Gaussian random variable

$$\begin{aligned} \mu_k &\triangleq \mathsf{M}(k,\cdot)\mathbf{b} \\ r_k &= \mathsf{M}(k,\cdot)\mathbf{b} + \sigma n_k = \mu_k + \sigma n_k \\ R_k &\sim \mathcal{N}(\mu_k, \sigma^2), \end{aligned} \tag{9}$$

where $n_k$ is the current realisation of the noise for user $k$.

The optimal detector applies the MAP decoding rule, i.e.

$$\hat{\mathbf{b}} = \arg\max_{\mathbf{b}\in\mathcal{B}} \; p(\mathbf{b}|\mathbf{r}) = \arg\max_{\mathbf{b}\in\mathcal{B}} \; p(\mathbf{b}, \mathbf{r}),$$

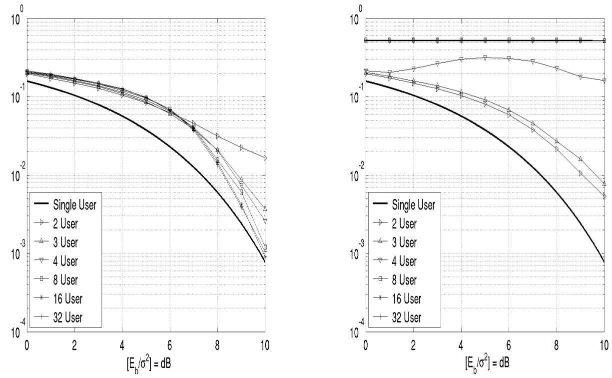
with the joint probability being

$$\begin{aligned} p(\mathbf{b}, \mathbf{r}) &= p(\mathbf{b})p(\mathbf{r}|\mathbf{b}) \\ &= p(\mathbf{b})p(r_1|\mathbf{b}) \prod_{k=2}^{n} p\big(r_k|r_1, \ldots, r_{k-1}, \mathbf{b}\big) \\ &= p(\mathbf{b})p(r_1|\mathbf{b}) \prod_{k=2}^{n} p\big(r_k|\mu_1 + \sigma n_1, \ldots, \mu_{k-1} + \sigma n_{k-1}, \mathbf{b}\big) \\ &= p(\mathbf{b})p(r_1|\mathbf{b}) \prod_{k=2}^{n} p\big(r_k|\sigma n_1, \ldots, \sigma n_{k-1}, \mathbf{b}\big) \qquad (10) \\ &= p(\mathbf{b}) \prod_{k=1}^{n} p\big(r_k|\mathbf{b}\big), \qquad (11) \end{aligned}$$

where (10) holds because $\mathbf{b}$ defines $\mu_k$ by (9) and equation (11) holds because the noise samples are independent by assumption. With the AWGN model, (11) expands to

$$\begin{aligned} p(\mathbf{b}, \mathbf{r}) &= p(\mathbf{b}) \prod_{k=1}^{n} p\big(r_k|\mathbf{b}\big) \\ &= p(\mathbf{b}) \big(2\pi\sigma^2\big)^{-n/2} \exp\left(-\frac{1}{2\sigma^2}\sum_{k=1}^{n}(r_k - \mu_k)^2\right), \end{aligned}$$

and because the input symbols $\mathbf{b} \in \mathcal{B}$ are uniformly distributed




(a) Flip mask (b) No mask

Fig. 3. Bit error rate results with and without a flip mask using the parallel iterative CBC receiver (synchronised system, no power control, 10 iterations, block length $l_b = 20$ bits)

by assumption, the MAP decoding rule finally becomes

$$\begin{aligned}\hat{\mathbf{b}} &= \arg\max_{\mathbf{b}\in\mathcal{B}} \ \frac{1}{|\mathcal{B}|}\left(2\pi\sigma^2\right)^{-n/2}\exp\left(-\frac{1}{2\sigma^2}\sum_{k=1}^{n}(r_k-\mu_k)^2\right)\\ &= \arg\min_{\mathbf{b}\in\mathcal{B}} \ +\frac{1}{2\sigma^2}\sum_{k=1}^{n}(r_k-\mu_k)^2\\ &= \arg\min_{\mathbf{b}\in\mathcal{B}} \ \|\mathbf{y}-\mu_k\|\,. \qquad (12)\end{aligned}$$

The practical relevance of this brute force method is very limited due to the computational cost even for very small matrices but in the next section it will be a useful tool for comparative reasons.

## IV. BER and EXIT Chart Analysis

The fundamental idea of IDMA is that every user uses the same repetition code but a different chip level interleaver. Using PIC, the performance heavily depends on whether or not a mask was used. Figure 3(b) shows the BER performance after 10 iterations for an IDMA system with (figure 3(a)) and without a flip mask (figure 3(b)), using the iterative chip-by-chip (CBC) detection approach from [2] with PIC, but with serial interference cancellation (SIC) the performance is similar to figure 3(a) (not shown here). The results were obtained for:

- repetition coding only, no additional outer channel code
- no channel, only AWGN distortion
- fully loaded, i.e. code rate of repetition code $r = 1/n$.

To get further insight into the problem we used extrinsic information transfer (EXIT) charts proposed in [10, 11] to analyse the convergence behaviour of concatenated codes. Instead of two concatenated codes the receiver has an elementary signal estimator (ESE) block which is basically a soft interference cancellation algorithm and a repetition decoder (despreader) block. Figure 4 shows the iterative CBC model for user $k$, where $R$ is the received data as in Figure 2, and the two terms $I_E$ and $I_A$ relate the mutual information of the data

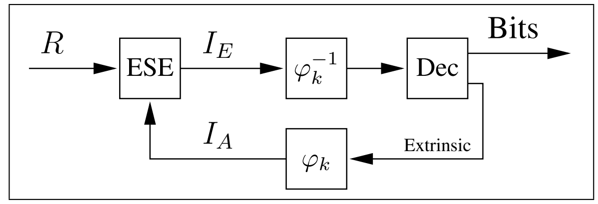
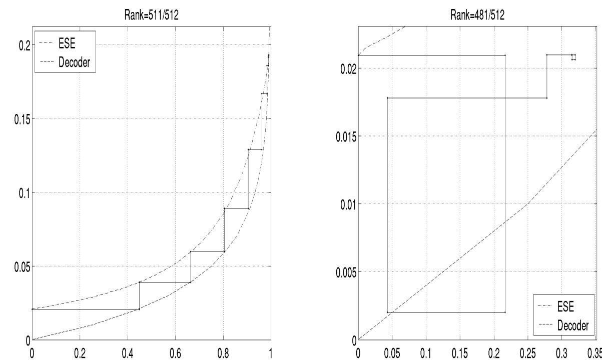



Fig. 4. Structure of iterative CBC receiver for user $k$. The ESE is also fed by the extrinsic information of all other users (not shown here).




(a) With flip mask (b) Without mask

Fig. 5. EXIT chart for $n = 32$ users, code rate $r = 1/32$, interleaver length $l_b = 16$ bits (512 chips) and SNR=10dB. The $x$ and $y$ axis show $I_E$ and $I_A$ respectively (see figure 4)

bits $B$ to the output of the ESE and decoder respectively. The probability distribution to compute $I_E$ and $I_A$ were obtained by Monte-Carlo simulation.

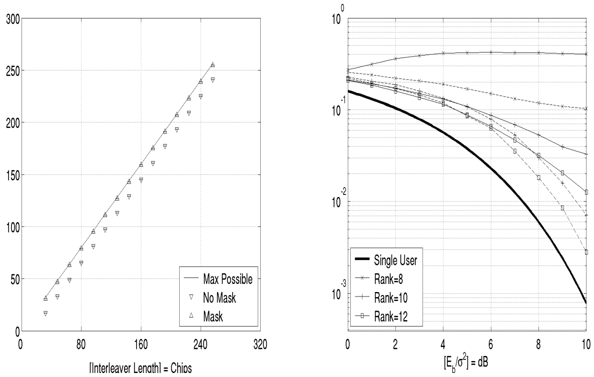
Figure 5 shows the convergence behaviour for $n = 32$ users, code rate of the repetition encoder $r = 1/32$, interleaving over $l_b = 16$ bits (512 chips) and SNR=10dB. With the flip-mask (figure 5(a)) the mutual information over the iterations stays tightly within the predicted performance but neglecting the mask (figure 5(b)) the mutual information is spiralling around the origin.

These system can be represented by system matrices of $\dim(\mathsf{G}) = 512 \times 512$ and one notable difference of the used matrices is the rank $\rho$ – with a flip mask the rank was $\rho = n - 1 = 511$ (figure 5(a)) and without mask only $\rho = n - 31 = 481$ (figure 5(b)).

## V. Repetition Coding

In Section II it was shown how to represent any synchronous IDMA transmitter with a matrix model. Here we focus on the structure of the system matrix $\mathsf{G}$ induced by the repetition coding and interleaving. The motivation for this investigation is to shed some light on a yet unsolved performance issue when using parallel soft interference cancellation and to link it to the matrix rank.

In terms of the system matrix $\mathsf{G}$, the only notably difference between the two schemes is that $\mathsf{G} \in \{0, +1\}$ without a mask and $\mathsf{G} \in \{-1, 0, +1\}$ with a mask. For instance the system




(a) Average Rank (b) BER

Fig. 6. The left figure shows the average rank of systems with and without a flip mask for $n = 16$ user and different interleaver lengths. The right figure compares the performance of the optimal decoder (dashed lines) and the iterative decoder (continuous lines) for $n = 4$ users and interleaving over $l_b = 3$ bits (12 chips).

matrix from the example above with and without flip mask is

$$\mathsf{G}_{\text{flip}} = \begin{bmatrix} +1 & 0 & +1 & 0 \\ -1 & 0 & 0 & -1 \\ 0 & +1 & 0 & +1 \\ 0 & -1 & -1 & 0 \end{bmatrix} \quad \mathsf{G} = \begin{bmatrix} +1 & 0 & +1 & 0 \\ +1 & 0 & 0 & +1 \\ 0 & +1 & 0 & +1 \\ 0 & +1 & +1 & 0 \end{bmatrix}.$$

With the additional {-1} element the matrix is well balanced and as shown by simulation, the average matrix rank is much higher. Note that the equalities (5) to (7) are not affected by the additional element.

In figure 6(a) the average rank of $\mathsf{G}$ for $n = 16$ user and code rate $r = 1/16$ is depicted. The height of the horizontal bar at each marker shows the standard deviation which is de facto zero. The empirical results indicate that the flip mask almost surely produces matrices that are rank deficient by at most 1 (i.e. $\rho \geq n - 1$), whereas neglecting the flip-mask results in severely rank deficient matrices.

Figure 6(b) compares the performance of the optimal decoder (12) with the iterative approach from [2]. Due to the exponential complexity of the optimal receiver with respect to the interleaver length, only a very small system with $n = 4$ users, code rate $r = 1/4$ and interleaving over $l_b = 3$ bits (12 chips) was considered which results in a $\dim(\mathsf{G}) = 12 \times 12$ matrix. None of the systems used a flip-mask but rather each user uses a randomly picked mask to produce matrices with different rank numbers. The general trend is that the performance degrades with the rank and that the optimal decoder always outperforms the iterative approach (irrespective of whether SIC or PIC is used). It was observed that for reasonably large systems the SIC method is hardly affected by the used mask and that for a flip mask, SIC and PIC perform equally well.

Note that for a given rank $\rho$ the results in figure 6(b) represent the performance of just a single matrix instantiation and is not an average result.

## VI. Conclusion

We showed how every synchronised IDMA signal can be described by a system matrix $\mathsf{G}$ and reduced the IDMA block diagram representation to the completely generic and very compact system model $\mathbf{Z} = \mathsf{G}\mathbf{B}$, with $\mathbf{B}$ being the source bits. Furthermore it was shown that the resulting matrices are extremely sparse and a measurement for the sparseness was derived. With this alternative yet equivalent system description additional analysis methods based on (sparse) matrix theory can be applied to further investigate and optimise the performance of the system.

Using BER and EXIT charts we showed that systems without a flip-mask using PIC are not converging at all. An empirically rank analysis indicated that such systems are always heavily rank deficient, whereas systems using a flip mask are almost surely of full rank or deficient by at most 1. Using SIC, the performance is not affected by the mask choice and therefore it can be concluded that indistinguishable IDMA signals due to a low rank occur very rarely, yet using a flip mask greatly reduces this risk for no cost.

At last the optimal receiver for this system model was derived and compared to the iterative receiver. As expected, the optimal decoder performs slightly better but for an unbearable complexity. Both receivers were used on rank deficient systems and it was shown that performance and rank are weakly linked for very small systems (matrices).

## References


[1] R. Mahadevappa and J. Proakis, "Mitigating multiple access interference and intersymbol interferece in uncoded CDMA systems with chip-level interleaving," *IEEE Trans. on Wireless Commun.*, vol. 1, no. 4, pp. 781–792, Oct. 2002.

[2] L. Ping, "Interleave-division multiple access and chip-by-chip iterative multi-user detection," *IEEE Commun. Magazine*, pp. S19–S23, Jun. 2005.

[3] P. A. Hoeher and H. Schoenreich, "Interleave-division multiple access from a multi user theory point of view," in *Turbo Coding 2006 Conference*, Munich, Germany, 3-7 April 2006.

[4] L. Ping, L. Liu, K. Wu, and W. Leung, "On interleave-division multiple-access," in *IEEE International Conference on Communications*, vol. 5, 20-24 June 2004, pp. 2869–2873.

[5] L. Ping, L. Liu, and W. Leung, "A simple approach to near-optimal multiuser detection: interleave-division multiple-access," *Wireless Communications and Networking Conference*, vol. 1, pp. S391–S396, 16-20 March 2003.

[6] L. Ping, L. Liu, K. Y. Wu, and W. K. Leung, "Interleave-division multiple-access," 2005, submitted to IEEE Trans. on Wireless Commun.

[7] L. Ping and L. Liu, "Analysis and design of IDMA systems based on SNR evolution and power allocation," in *IEEE Veh. Tech. Conference*, Sept. 2004, pp. 1068–1072.

[8] K. Li, X. Wang, and P. Li, "Analysis and optimization of interleave-division multiple-access communication systems," *Acoustics, Speech, and Signal Processing, Proceedings, ICASSP '05*, vol. 3, p. S917, 18-23 March 2005.

[9] H. Wu, L. Ping, and A. P. A, "User-specific chip-level interleaver design for IDMA systems," *Electronics Letters*, vol. 42, pp. S233–S234, Februar 2006.

[10] S. ten Brink, "Convergence behavior of iteratively decoded parallel concatenated codes," *IEEE Transactions on Communications*, vol. 49, no. 10, pp. 1727–1737, Oct 2001.

[11] F. Brannstrom, L. Rasmussen, and A. Grant, "Convergence analysis and optimal scheduling for multiple concatenated codes," *IEEE Transactions on Information Theory*, vol. 51, no. 9, pp. 3354–3364, Sep 2005.