

Using the classical theory of delay line design [1, pp. 800-808], but based upon image admittances in place of image impedances, we obtain a delay line as a cascade of  $m$ -derived sections as shown in Fig. 1. Customarily for wide frequency usage  $m=1.27$  for internal sections, while for matching to source and load  $m=0.6$  for terminating sections, with  $R=\sqrt{L/C}$ . Ignoring the delay of the terminating sections the delay to the  $k$ th tap is approximately [1, p. 805]

$$t_k = km\sqrt{LC} \quad (1)$$

from which we determine

$$L = \frac{t_k R}{km}, \quad C = L/R^2. \quad (2a)$$

From (2) we note that if we desire to keep  $C$  constant then the  $k$ th delay can be varied by simultaneously varying  $L$  and  $R$  such that  $L/R^2$  remains constant, thus

$$L = \frac{1}{C} \left( \frac{t_k}{km} \right)^2 \quad (2b)$$

determines  $L$  for a given capacitor size  $C$  and delay time  $t_k$ .

To vary  $L$  we first observe that the circuit of Fig. 2(a), which is a special case of a previous circuit [6], and which has also been described by Holt and Taylor [8] in the constant parameter case, is described by

$$v_1 = \frac{R_{b1}}{R_{a2}} v_2 - R_{b1} c \frac{dR_{b2} i_2}{dt} \quad (3a)$$

$$i_1 = - \frac{R_{b2}}{R_{a1}} i_2. \quad (3b)$$

Consequently the equality of Fig. 2(a) with 2(b) results when  $R_{b2}/R_{a1} = R_{b1}/R_{a2} = 1$  and the equivalent inductance can be varied by varying  $R_{b1}$ . But  $R_{b1}$  can be easily electronically varied [1], as can the other resistors  $R$ , in fact such that  $C=L/R^2$  remains constant.

When  $m$  is set equal to its customary value of 1.27, the capacitors shunting the inductors will be *negative*; however, the capacitor  $\pi$ -network is always realizable by coupled capacitors [6]. The main sections are then realized by connecting the coupled capacitors in parallel with the circuit of Fig. 2(a), as shown in Fig. 3. A similar structure of course holds for the terminating half sections.

Several comments are worthwhile. First, Fig. 3 is imminently realizable by integrated circuit techniques. For such a realization the original gyrator [5] is most suitable for the lower-right gyrator because of the presence of the capacitor, while a modified bias structure under investigation should allow combining the two lower gyrators. However, the remaining two gyrators would preferably be of the more recent direct-coupled type [9], [10]. Since thousands of sections could be cascaded in integrated form the circuit should allow for rather large delays. In addition, it can be noted that where one is interested in delaying signals of audio frequencies [4], the gyrator realization should be considerably cheaper and smaller than the corresponding normal passive reciprocal realization. For instance to realize delays of about 0.1 ms per section of a line in the normal reciprocal passive circuit form requires several inductors of the order of 10-100 mh for a 1 k $\Omega$  image impedance. In gyrator form the entire circuit can be integrated, with considerable savings in size, weight, and cost.

If all that is desired is delay, without taps, then modern filter design can be applied to synthesize a ladder structure similar to Fig. 1 [11], and the inductor replacements of Fig. 2 made. By relaxing the  $R_{b2} = R_{a1}$  constraint of Fig. 2(b), but choosing  $R_{a1}$  very large, one can also obtain essentially reflectionless transmission. This results from the nonreciprocal nature of the resulting structure, or noting that  $i_1 = 0$  results from  $i_2 \neq 0$  when  $R_{a1} \approx \infty$ , (3b).

In actual fact, variation of the terminating resistors does not seem too critical, as indicated by previous types of practical variable delay lines [12]. Because the present variable gyrators [5], [9], [10] are limited in frequency response, the circuits for Fig. 3 are limited to

### A Tapped Electronically Variable Delay Line Suitable for Integrated Circuits

In electronic [1, p. 83] and sampled-data systems [2, p. 76] the use of delay lines is frequent and their design important. Often it is important to consider tapped delay lines, as in distributed amplifiers [3, p. 149] or adaptive communication systems [4, p. 25]. Here we show how with fixed taps a variable delay per section can be implemented. The theory rests upon that of a time-variable gyrator [5] and associated circuitry [6]. Possible applications are to the design of variable-gain distributed amplifiers and to the modeling of variable media, as the ionosphere for radar studies [7, p. 69].

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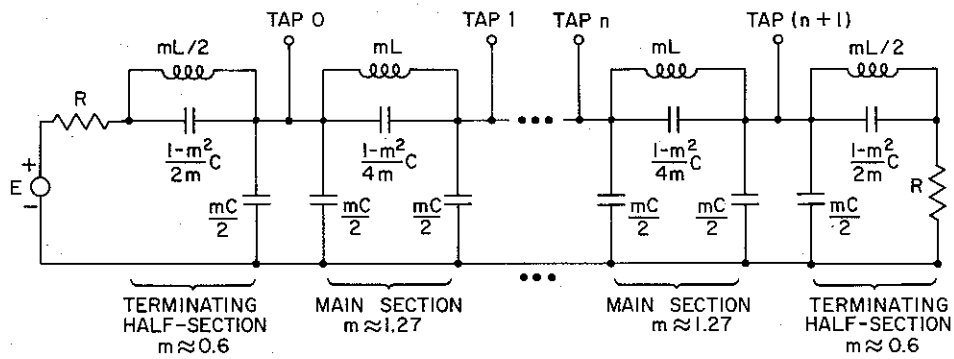


Fig. 1. Admittance designed delay line.

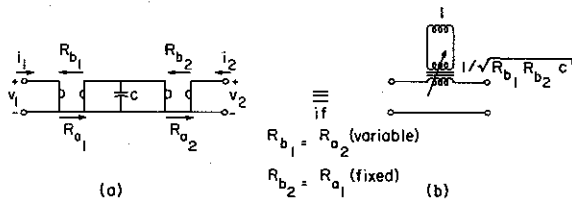


Fig. 2. Variable inductor realization.

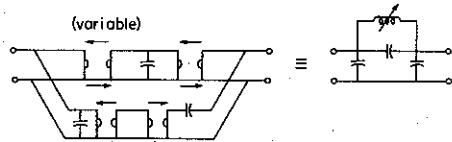


Fig. 3. Main section realization.

under 10 Mc/s at this date. Likewise it should be pointed out that (1) is really valid only for somewhat stationary values of  $L$  and thus for rapid and continuous variations in delay a new theory needs development.

The idea of converting to an admittance formulation stems from a similar use of admittances to obtain RC grounded gyrator realizations of all Darlington sections by H. J. Orchard [13].

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