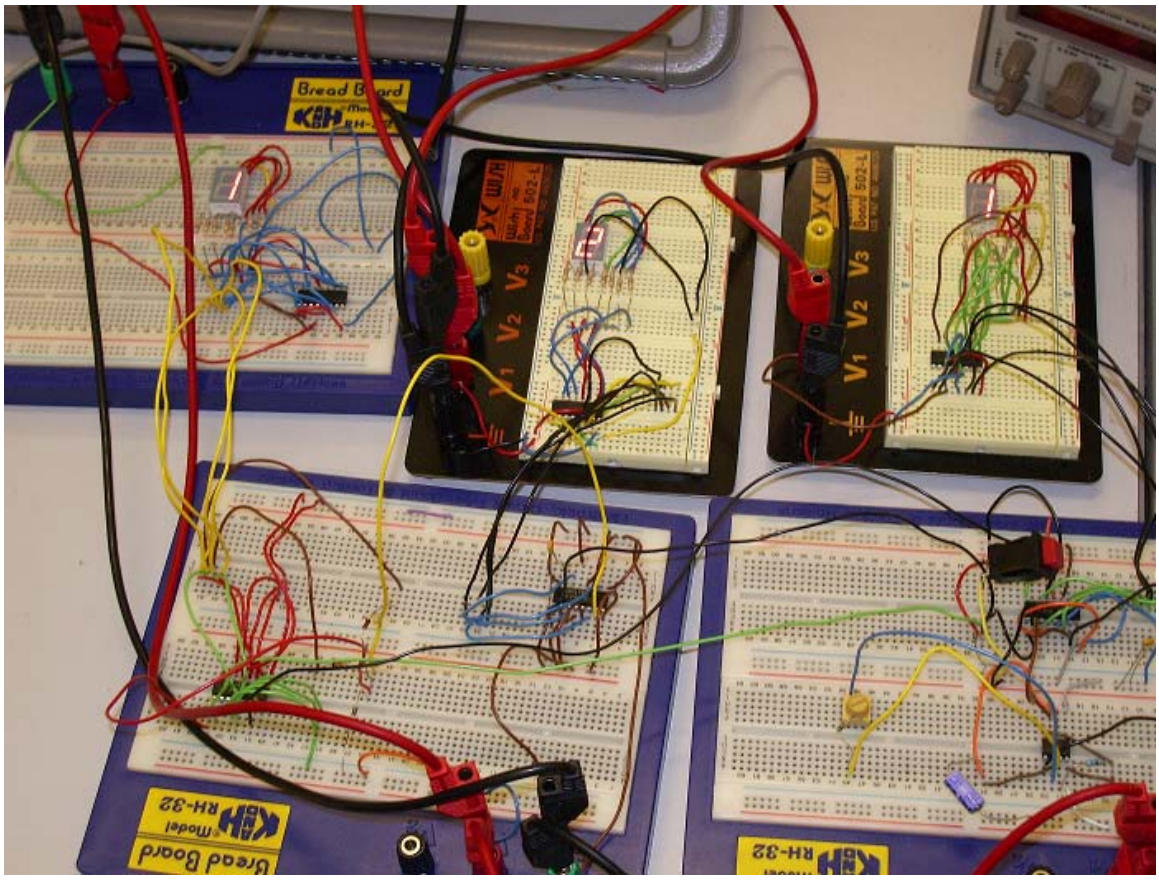
A Digital Timer Implementation using 7 Segment Displays



Group Members: Tiffany Sham u2548168
Michael Couchman u4111670
Simon Oseineks u2566139
Caitlyn Young u4233209

Subject: ENGN3227 - Analogue Electronics
Lecturer: Salman Durrani
Date Due: 24/10/06

Table of Contents

1.0 Abstract

In this report, the design and implementation processes of a digital timer circuit based on the 555 timer are documented. The initial design criteria for the project were 1. To have a three digit output, 2. To have the circuit count from 0:00 to 9:59 and 3. To include either an op-amp or 555 timer. Research was conducted into similar analogue electronic circuits and a suitable starting point of a digital die was identified. Using this starting point, a digital timer circuit was designed using a 555 timer, BCD4510 binary counters and 7 segment display outputs. The proposed circuit was modelled using PSpice and Digital Works, showing that the concepts used in the design were sound. The circuit was then implemented and tested on breadboard before a PCB implementation was prepared.

2.0 Background

Timers were originally designed to fulfill a need in industry for a means of keeping time on certain devices. Originally, these timers were mechanical devices and used clockwork mechanisms as a means of keeping a regular time (*Timer*, 2006). The invention of two electromechanical timer designs allowed for more precise time measurement. The first uses the principle of heat expansion to increase the temperature of a metal finger made of two different metals with differing rates of thermal expansion (*Timer*, 2006). As electric current flows through the metal, it begins to heat and one side expands more quickly than the other which, in turn, moves the electrical contact away from an electrical switch contact. The second uses a small AC motor which turns at a predetermined rate due to the application of an alternating current (*Timer*, 2006).

Finally, digital timers were invented. Digital logic circuits are now so cheap that it has become a better investment to buy a digital timer than a mechanical or electromechanical timer. Individual timers are implemented with single chip circuits, similar to a watch (*Timer*, 2006). The 555 timer used in this project is a combination of a digital logic circuit and analogue components.

3.0 Theory

Electronics designers use 555 timers in timing circuits and the binary counter decimal (BCD) integrated counting circuits in order to implement a timer. Though programmable micro-controllers are more commonly used, a simpler solution for three or more digit timers. BCDs are also valid in this application.

3.1 555 timer

555 timers are integrated timing circuits which are used commonly as a source of clock pulses to drive subsequent timer circuits. They are analogue devices which can produce an oscillating and digital output. The IC can be configured to give an astable, period output or a monostable, single triggered output.

In the project circuit, the astable configuration is implemented. A square wave output is generated with the configuration shown below, mainly by the use of an external capacitor charging and discharging. Comparator circuits internal to the timer, compare the supply voltage and capacitor charge to produce either a HIGH or LOW switching output. The duty cycle and frequency of the output pulses can be set using external resistors and a capacitor.

Frequency, f = 1.44/[(R1+R2)C]

Duty cycle = [(R1+R2)/(R1+2R2)]x 100%

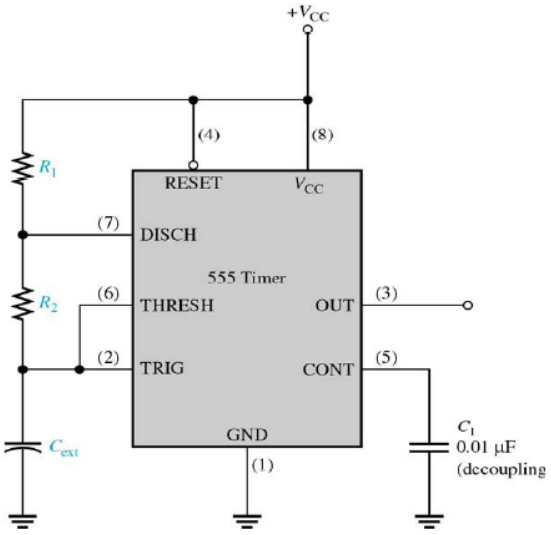


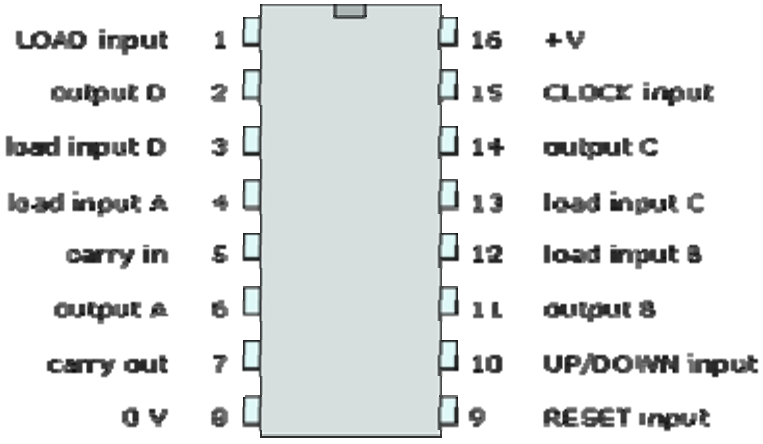
Figure 1: 555 Timer in Astable Arrangement

Very low tolerances are required for the components in order to have a very accurate counting circuit; thus 555 timers are not used in precise real world applications. However in order to demonstrate the timing principle, the 555 timer is a cheap alternative to other timing devices such as piezo electric crystals.

3.2 BCD4510 counters

BCDs are integrated CMOS transistor logic circuits. A BCD counter is an integrated circuit that counts when triggered by a clock input and expresses the count as a digital binary output. The BCD4510 counter is a four-bit output device which cycles through the numbers 0 to 9. The IC can count either up or down and the counter is synchronous meaning that the outputs change precisely together on each clock pulse. The outputs are labelled output A, B, C and D, with output A as the least significant bit. The outputs are denoted in bits due to the sequential clock pulses are shown in Table 1.

Figure 2: BCD4510 Pin Configuration



The BCD counts with a clock input, which is an input at pin 15 from a timer device such as the 555 timer. Pin 1 Load input (also known as preset) determines on which edge of the clock pulse the counter will count (either rising or falling edge). Pin 10 UP/DOWN input determines whether the circuit counts up or down- HIGH for up, LOW for down. In normal counting operation Load input, RESET and carry in should be low. When RESET is high it resets the count to zero. The clock input should be low when resetting. The counter can be set to count from a specified number by inputs into the load inputs A, B, C and D. The counters can be cascaded using carry in (pin 5) and carry out (pin 7). The carry out pin sends a HIGH signal when the counter changes between 0 and 9.

The internal circuitry of a BCD4510 includes a number of NOT and NAND gates and flip-flops. These devices are implemented with transistors, and make up the two circuit blocks, a parallel load circuitry to handle the inputs and an up/down counter.

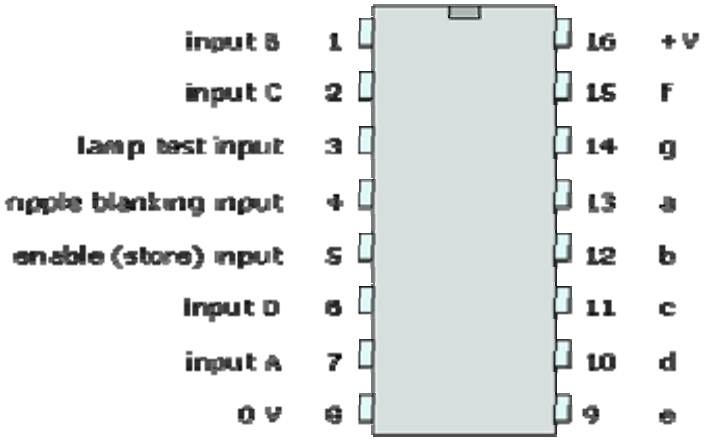
3.3 BCD4511 decoders

The BCD4511 decoder is a complementary IC to the BCD4510 counter and the seven segment display. It converts the logic inputs from the BCD4510 counter into an eight-bit output that drives the seven segment displays with the outputs a through to g.

Table 1: BCD outputs and corresponding digits

Clock Pulse	**BCD4510 output/ BCD4511 input**				**BCD4511 output**							**7-Segment Displayed Digit**
	D	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	0	0	0	0	0	1
2	0	0	1	0	1	1	0	1	1	0	1	2
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	1	1	4
5	0	1	0	1	1	0	1	1	0	1	1	5
6	0	1	1	0	1	0	1	1	1	1	1	6
7	0	1	1	1	1	1	1	0	0	0	0	7
8	1	0	0	0	1	1	1	1	1	1	1	8
9	1	0	0	1	1	1	1	1	0	1	1	9

Figure 3: BCD4511 Pin Configuration



The inputs A through to D accept the 4 bit the binary output from a BCD counter such as BCD4510. Lamp test input and ripple blanking input are LOW for normal operation. Lamp test input pin 3 causes the BCD to produce all HIGH on the outputs when it is LOW, to fully test the segment display. When ripple blanking input, pin 4, is LOW, all the outputs are LOW, blanking the segment display. The store input should be LOW for normal operation. When store is HIGH the displayed number is stored internally to give a constant display regardless of any changes, which may occur to the inputs.

Like the BCD4510, the 4511's internal circuitry consists of a number of NOT gates, AND gates and flip-flops. The main sections of the circuit include a latch circuit for the inputs connected to a decoder block that in turn is connected to a driver block and to the seven segment display outputs.

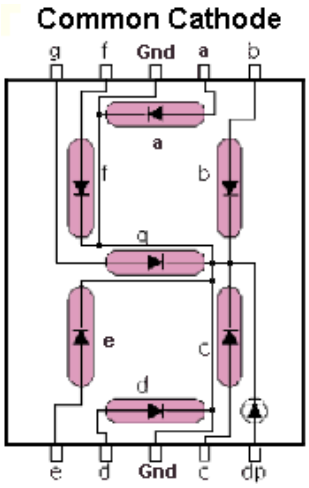
3.4 Seven segment displays

Seven segment displays are an arrangement of LEDs that simply accept a digital input to display a digit from 0 to 9. The digits are made up of seven individually illuminated slots to display the digits. The display can also illuminate a decimal point. Seven segment displays are one of the oldest electronic methods for displaying numeric information but also one of the simplest.

There are two types of seven segment displays, common cathode and common anode displays. In a common cathode display, the cathodes of the LEDs are joined together and the individual segments illuminated by HIGH voltages. In a common anode display, the anodes of the LEDs are joined together and the individual segments illuminated by LOW voltages. In this project, common cathode seven segment displays were used, with the joined cathode connected to ground.

Figure 4: Common Cathode Display Layout and Corresponding Pin Numbers

Segment	Pin number
a	7
b	6
c	4
d	2
e	1
f	9
g	10
GND	3,8
Decimal point (DP)	5



3.5 Diode logic gates

Logic gates can be implemented with the use of diodes. In the project circuit, an AND gate is created with two diodes, to send a signal to the minutes counter to count when the tens of seconds counter reaches 6.

Figure 5: AND gate

If either diode input is LOW, the diode will forward bias and conduct to produce an output of LOW. If the both the inputs are grounded or HIGH, the AND gate output will be HIGH.

4.0 Design

The design specifications for this project were as follows:

- Design must contain an op-amp, ADC, DAC or 555 timer.
- Have a three digit output.
- Have the circuit count from 000 to 959 then have it reset itself.

4.1 Top Level Design

The first step in the design of any complex circuit is a top level block diagram identifying the basic functions which must be performed. The following block diagram was prepared using the design specifications above as a guide:

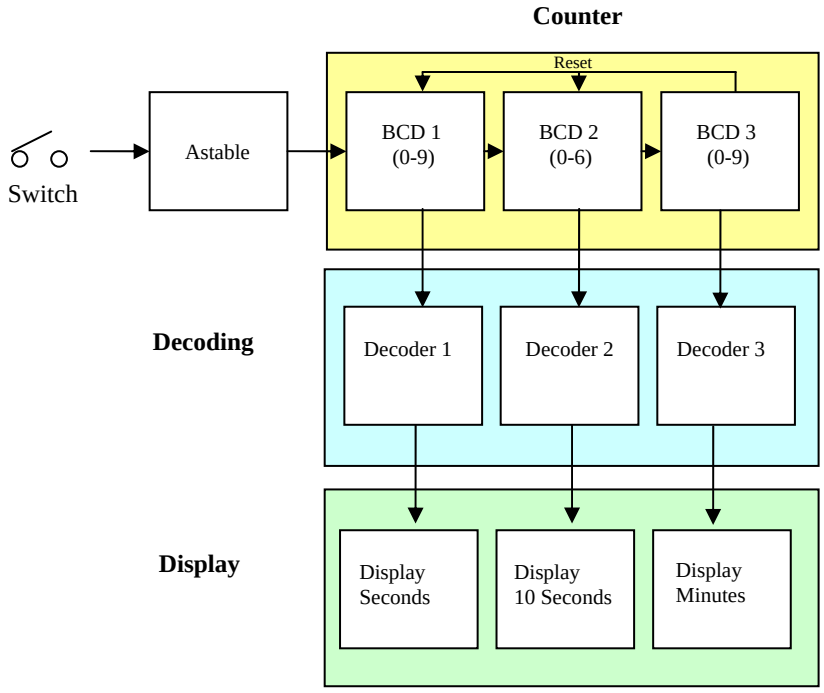


Figure 6 - Block Diagram

With the above diagram in mind, implementations of similar circuits were researched. The circuit shown in Appendix A Fig 1 was used as a starting point for the design as it contains parts of the astable, counter, decoding and display circuit blocks. From this starting point, other elements could be designed and integrated into a new circuit.

4.2 Lower level design

The original design for the project was for a single seven segment display timer counting from one to six. This was implemented using a 555 Timer in an astable configuration, a 4510 Binary Coding Decimal (BCD) counter, and a seven segment display (Appendix A Figure 1). As this circuit was straightforward to implement, a ten minute timing circuit was decided as a reasonable design to implement. The basic design from Appendix A was used as a building block for a cascaded timing circuit. The basic design in Appendix A was for a timer that counted from 1 – 6 then back to 1 again. This had to be changed in order to allow a ten minute timer to be produced.

The code conversion section of the basic design allows the counter to count from one to six then back again. It was removed and the BCD's were connected directly to their corresponding 4511 Seven Segment Decoding chips.

The 555 Timer remained the driver for the circuit with the pause switch being removed so as to simplify that particular part of the circuit. The 15 kΩ resistor was replaced with a 10 kΩ resistor in series with a 1 - 5 kΩ variable resistor, so the frequency of the 555 Timer could be modified to produce a 1 Hz signal (Appendix A, Figure 2).

The 555 Timer output was then connected to the clock input of the first BCD (BCD1). BCD1 was configured to count from 0 – 9 then reset itself automatically, counting the seconds in the timing circuit. When BCD1 resets itself it sends a pulse from pin 7 or the carry out pin. A wire from pin 7 was then connected to the clock input of the second BCD (BCD2), so when BCD1 reset itself the pulse sent through pin 7 would trigger the clock input of BCD2.

BCD2 counts the tens of seconds in the circuit, so in order to have it count properly the timer was limited to count to five before being forced to reset on the next input pulse from BCD1. This was achieved using an And gate connected to the second and third bit output terminals of BCD2. As the binary representation for six is 0110, when both the second and third bit was high the And gate allowed the reset pin of BCD2 to be triggered, making the second seven segment display go straight from five to zero.

The final BCD, BCD3, counts the minutes in the timing circuit. This was triggered using the same And gate that triggered the reset of BCD2. As the reset of BCD2 only triggered when it reached six, it seemed reasonable to get the And gate to trigger the clock input of BCD3 at the same time, removing the need for any extra circuit parts.

The outputs of the BCD's were then connected to 4511 chips. Then the 4511 chips were connected to the seven segment displays. As an addition to the circuit a reset switch was attached to the reset pins of all of the BCD's, when compressed the switch sends a continuous high voltage signal to the BCD's preventing them from counting until the switch is off.

For the full schematic see Appendix A, Figure 3.

The Seven Segment Displays were chosen as the desired output of this circuit for their compact packaging and ease of implementation. An LCD display was considered for an alternate form of output but their expense and with the seven segment displays it was easier to see the output.

The 555 Timer was chosen as the driver for this circuit as it conformed with the ENGN3227 course content. Also, the 555 Timer is one of the most accurate IC timers developed. Combined with its low cost, the 555 Timer was deemed the most appropriate timer that could be readily attained.

4.3 Simulation

A PSpice simulation was used to fine tune the component values of the astable section of the design in order to achieve a clean 1 Hz square wave. The schematic and output are

given in Appendix A fig 5. As a 1 Hz waveform could not be obtained using combinations of standard resistors and capacitors, the decision was made to include a potentiometer in the implementation of the circuit to fine tune the 555 timer output frequency.

A “proof of concept” simulation was also created using Digital Works, to show that the digital logic used in the circuit was sound. Macros for BCD4510 counters were unavailable in the Digital Works simulation package, so flip-flops were used instead to simulate their operation. This design is shown in Appendix A fig 4.

5.0 Implementation

Implementation of the digital timer project took place between the 12th and 16th of September, 2006. The digital timer circuit was the first project to be successfully implemented on breadboard, due in a large part to the logical construction and troubleshooting process outlined in the following sections.

5.1 Construction Process (Breadboard)

This circuit can be split into several discrete, individually testable blocks, as shown in Figure 6, the block diagram. In order to expedite the implementation of the circuit, circuit blocks were built and tested individually on breadboard and integrated with the circuit to build up to the full 3 digit implementation. The circuit was executed in the following order:

1. 555 Timer (Appendix D part II)
2. Test of 555 timer circuit using oscilloscope
3. BCD 1 (Seconds) constructed
4. One 7 segment display output built
5. 555 timer, BCD 1 and first 7 segment output connected together
6. Visual test of 555 timer, BCD 1 and 7 segment output
7. Remaining 7 segment display outputs built
8. Test of remaining 7 segment display outputs by placing them in the circuit and testing as per (6).
9. BCD 2 (10 Seconds) constructed
10. 555 timer, BCD 1 and 2, two 7 segment displays connected together
11. Visual test of circuit implemented in (10)
12. AND gate added to BCD to in order to reset after 0-5 count
13. Visual test of (12)
14. BCD 3 (Minutes) constructed
15. 555 timer, BCD 1, 2 and 3, three 7 segment displays connected together
16. Visual test of (15)
17. Reset switch added
18. Operation of final circuit tested visually and with oscilloscope

An oscilloscope was connected to the input of each BCD following the completion of steps 5, 10 and 15. These signals are shown below in Appendix B.

The implementation process followed a logical progression, integrating separate blocks into the growing circuit once normal operation of existing components was established. Starting with a full 1-9 seconds count and testing by observing the output from the 7 segment display enabled the group to show that the 555 timer, BCD4510, BCD4511 and 7 segment displays were all compatible before proceeding with more complex interconnections.

The most challenging task in implementing this circuit was properly connecting the three BCD4510 ICs. As these ICs were not included in any available simulation packages, troubleshooting of possible logic errors in the design of the circuit had to be done during implementation using the relevant datasheets. Building and testing all display circuits before connecting the BCD4510 ICs meant that possible logic or wiring errors were isolated to the new BCD4510 being added to the circuit.

5.2 Construction process (PCB)

Unfortunately the method described in section 5.1 could not be used in the construction of the PCB. The design was finalised using EAGLE and then sent for etching by an external company on a double layer board, making detection and correction of any layout errors difficult.

The construction process using the PCB involved soldering components to the nominated positions on the PCB. All components were labelled in the design notes and on the PCB itself. Due to the nature of the layout, all components had to be connected before any testing could take place. Because of the complexity of the connections between ICs, a modular design may have been more appropriate in this case.

5.3 Troubleshooting

5.3.1 Breadboard Troubleshooting

During the troubleshooting phase, problems were encountered at the testing steps 5, 10 and 15.

Step 5

1. The single display occasionally skipped digits. This was due to a wiring error in the astable section. Once the wiring error was corrected, normal operation of the “seconds” counter was established.

Step 10

1. The second display oscillated between “2” and “6”. The diodes D1 and D2 on Appendix A Fig 3 had been connected incorrectly.
2. The second display counted twice as fast on even digits than on odd digits. Voltage spikes on the input pin such as those shown on Appendix A Fig 6 were

thought to be causing this. Several decoupling capacitors were used to minimise the magnitude of the spikes.

Step 15

1. After the "reset" pins were connected together, the circuit no longer counted and an output of "000" on the 7 segment displays was observed. The reset switch had been inadvertently connected to the 9V rail and had locked the three counters in the "reset" state.

5.3.2 PCB Troubleshooting

As of the writing of this report, the PCB implementation of the digital timer is non-functional. Several factors may have contributed to the circuit problems:

- Short circuits either due to imperfections in PCB manufacturing or solder joints connecting tracks – Using a multimeter set to sound when an electrical connection was made, several overly large solder joints were found to be connecting tracks. These were removed using solder wick. Several holes were found to be connected to a neighbouring track. These connections were broken with a knife.
- Open circuits due to breaks in tracks. Again, tracks were tested using a multimeter. No track breaks were identified.
- Heat damage to components during the soldering process. Inputs and outputs of the various ICs were examined using an oscilloscope. As the output from the 555 timer did not appear as expected, this may be the principal cause of circuit failure.
- Errors in transcribing the breadboard design to PCB design using EAGLE. No transcription errors were identified on the schematic input to EAGLE, however due to the double sided PCB, errors in converting the schematic into a PCB layout were difficult to investigate.

6.0 Conclusion

Analogue electronics components were investigated and a 555 timer, a BCD counter, a BCD Decoder and a seven segment display were combined to form a digital timer circuit. Different methods were analysed to determine the best technique for creating an efficient timer until one was chosen and the circuit was designed. The chosen circuit was verified through simulation using PSpice and Digital Works. This design was then implemented and modified to suit the needs of the project. Problems were analysed and repaired where necessary until it was concluded that the circuit had met the design criteria of the project. Once the correct operation of the circuit was verified, a PCB implementation was designed in order to make the circuit more concise and more accurate.

The PCB implementation did not perform as planned. Time restrictions meant that only track connectivity issues on the PCB were investigated and while several problems were identified, correcting these issues did not lead to normal operation of the circuit.

7.0 Bibilography

1) Unknown, *Analogue Electronics*, 2006. Retrieved on 18/10/06 from en.wikipedia.org/wiki/Analogue_electronics
2) Science and Technology Encyclopaedia, *Electronics*, Unknown. Retrieved on 17/10/06 from http://www.answers.com/topic/electronics
3) Unknown, *Timer*, 2006. Retrieved on 17/10/06 from en.wikipedia.org/wiki/Timer
4) Phillips, *BCD Up/Down Counter*, Unknown. Retrieved on 12/10/06 from http://www.doctronics.co.uk/4510.htm
5) Phillips, *BCD to 7 segment Decoder*, Unknown. Retrieved on 13/10/06 from http://www.doctronics.co.uk/4511.htm
6) Unknown, *Interfacing to 7-Segment Numeric Displays*, Unknown. Retrieved on 14/10/06 from http://www.thelearningpit.com/lp/doc/7seg/7seg.html
7) Unknown, *Diode Logic*, 2006. Retrieved on 12/10/06 from http://www.play-hookey.com/digital/electronics/dl_gates.html

Appendix A

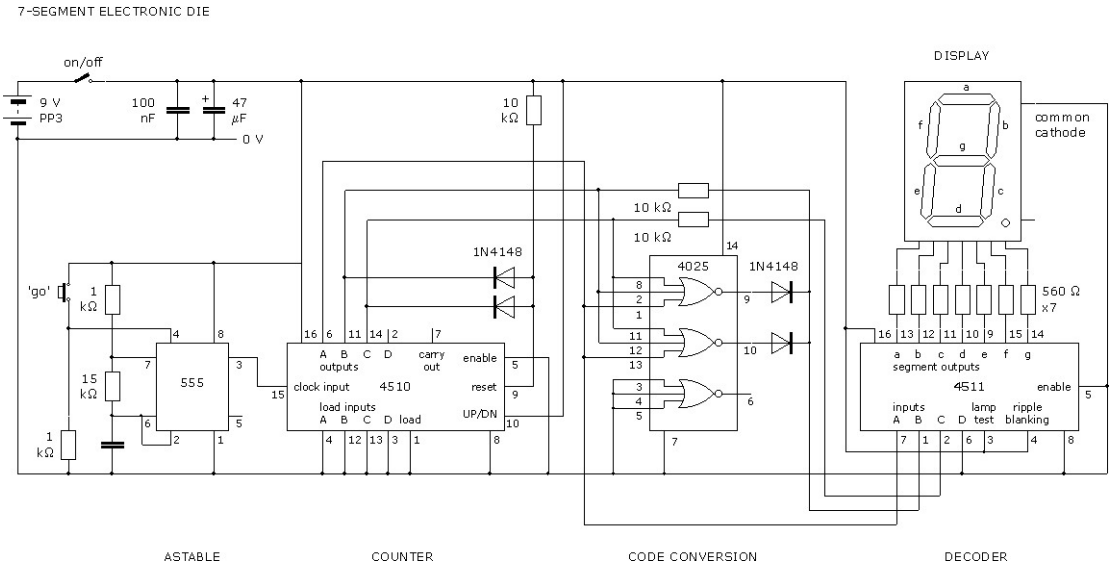


Figure 1: 7 Segment Electronic Die

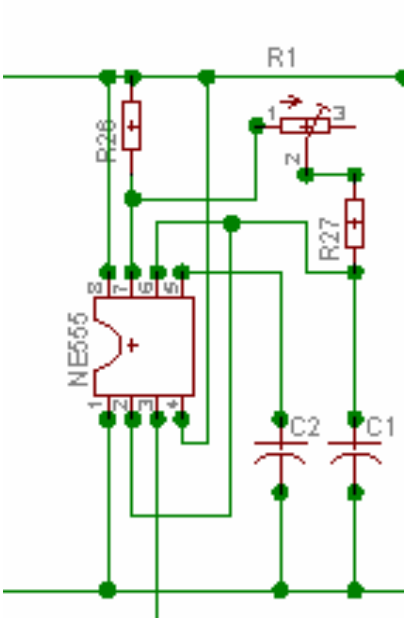


Figure 2: The 555 Timer Configuration

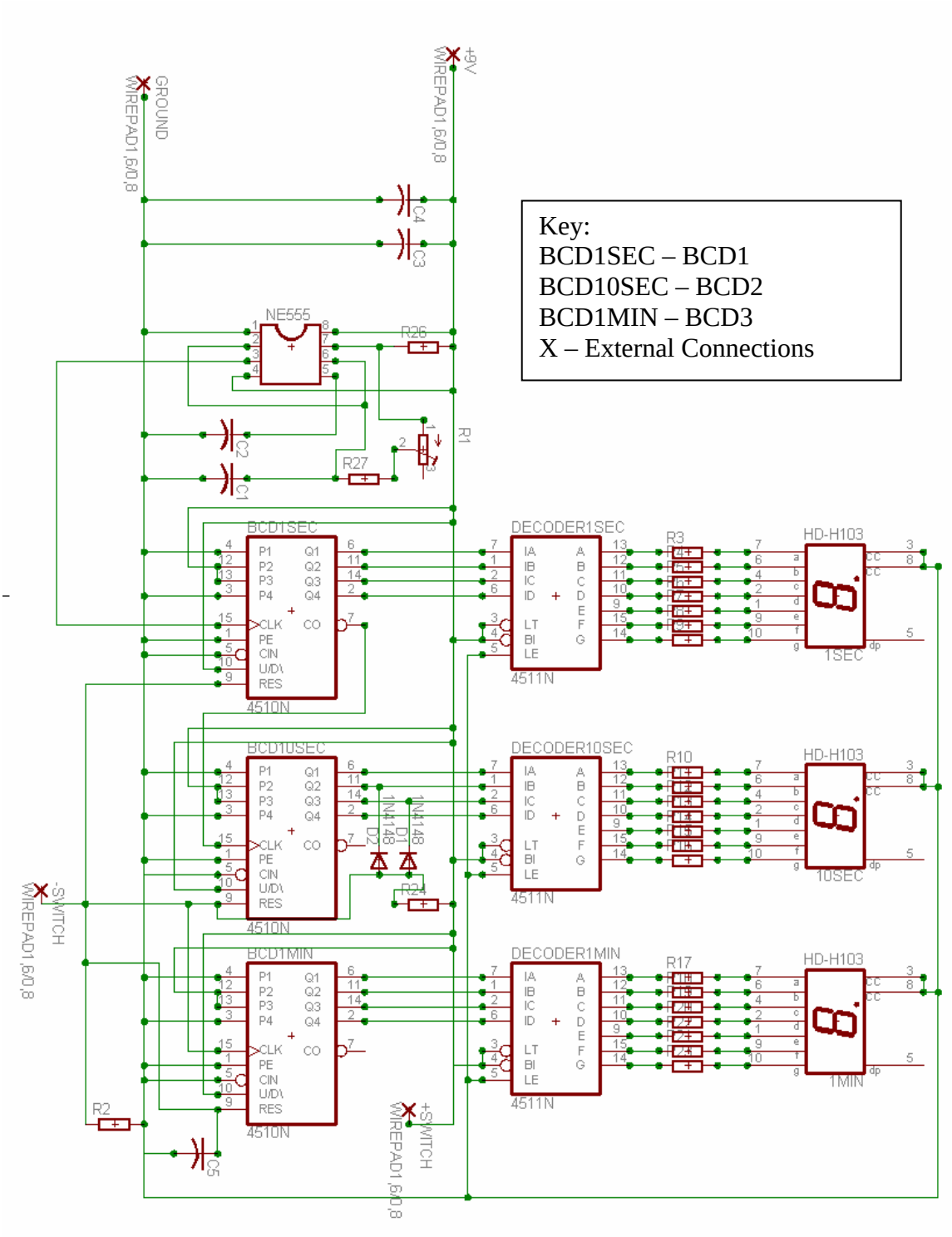


Figure 3: Schematic of the Digital Timer

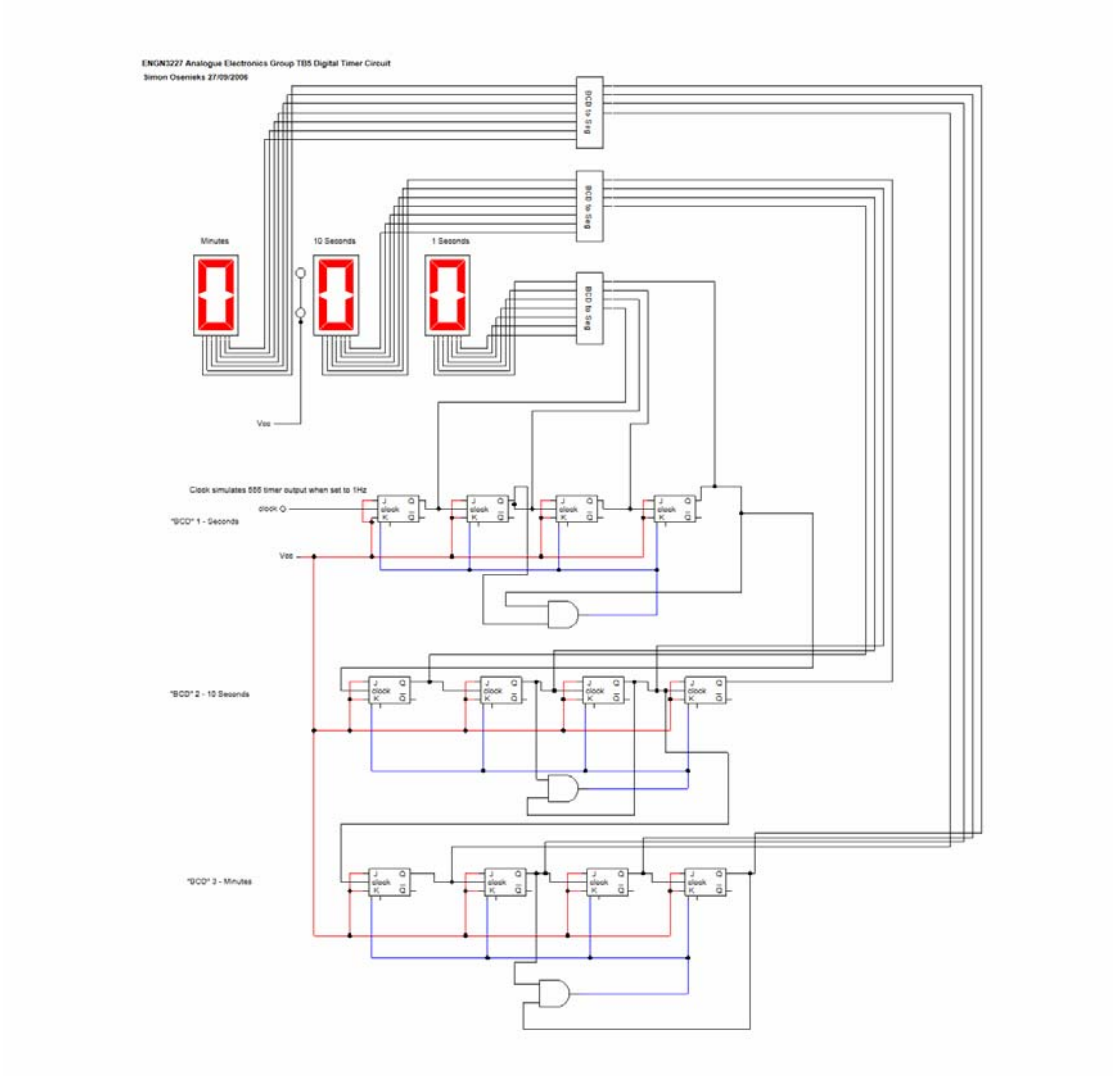


Fig 4 – Digital Works “Proof of Concept” Simulation

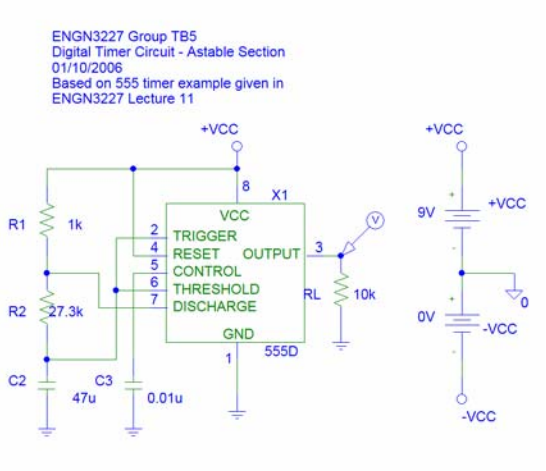


Fig 5 – PSpice schematic layout

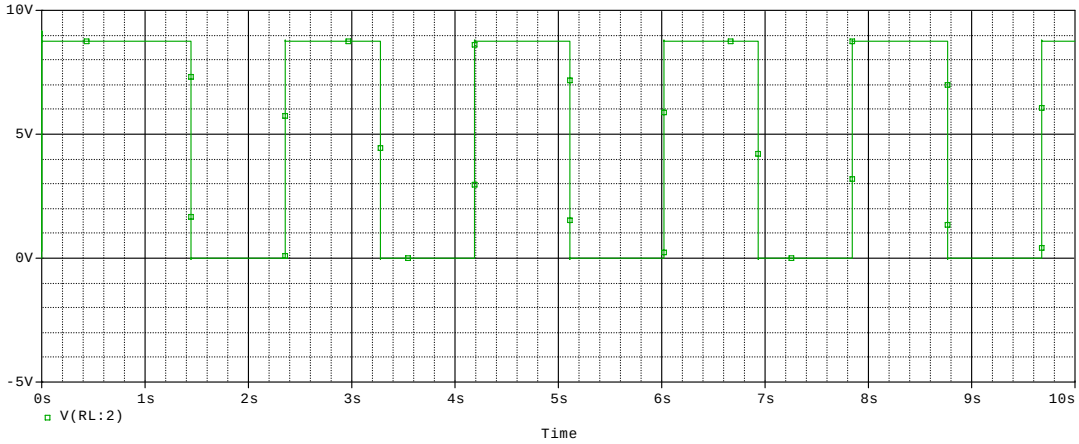


Fig 6 – Output across R_L from Fig 5. A signal approximating a 1Hz square wave can be observed after the transient charging of the capacitor (0s-1.5s) has occurred.

Appendix B – Oscilliscope outputs of Waveform

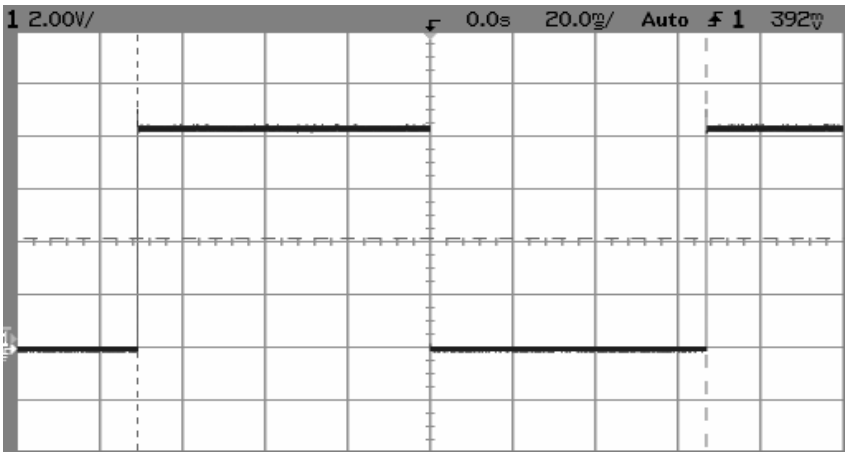


Fig (a) – Input to BCD1 (Seconds) – Step 5. The “seconds” frequency was set to 7.5Hz for testing purposes.

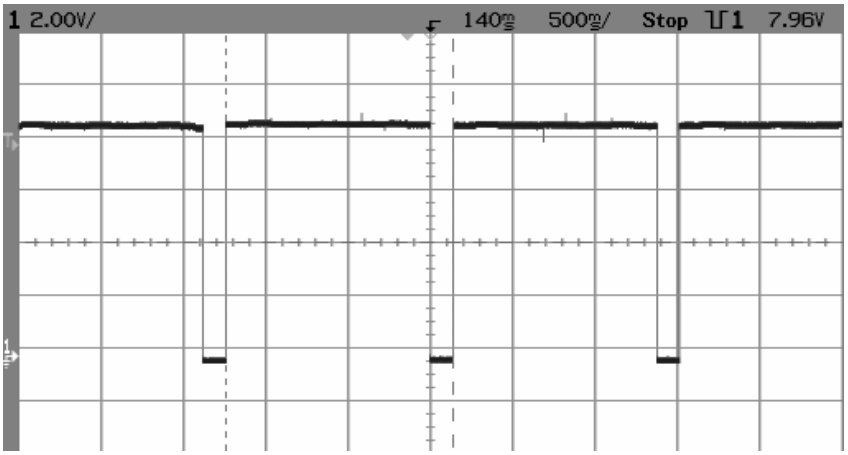


Fig (b) – Input to BCD2 (10 Seconds) – Step 10

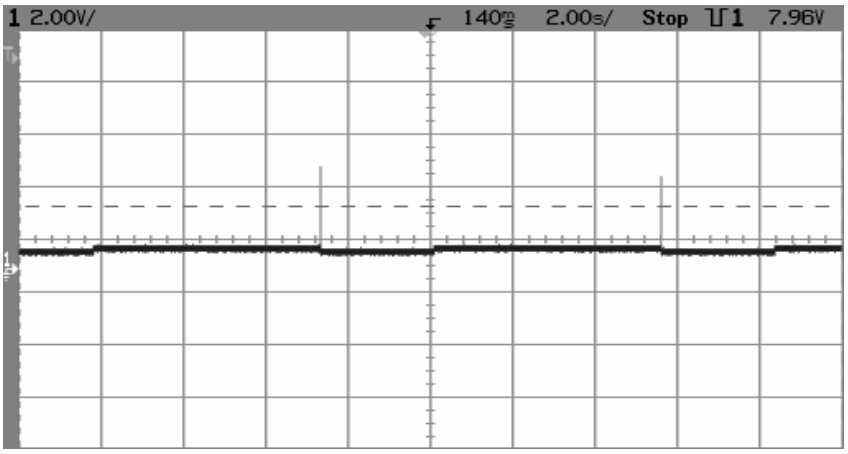


Fig (c) – Input to BCD3 (Minutes) – Step 15