ENGN3227
Analogue Electronics

Project Report: Metronome and Pitch Generator Circuit

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Abstract

A simple metronome circuit based on a 555 timer was constructed in the electronic simulation program, PSPICE, demonstrating the feasibility of the design concept. A more complicated circuit capable of functioning as a metronome or pitch generator was then successfully implemented on a breadboard circuit. This circuit uses a crystal oscillator circuit for frequency generation and a phase-locked loop for synthesis of other frequencies which can be set with counter switches. A printed circuit board was designed for the final implementation.

Introduction

The metronome is defined as "a device used to mark time by means of regularly recurring ticks or flashes at adjustable intervals" (1). It is usually used to keep a standard tempo (steady beat) throughout a piece of music and may be used in practice or performance of a musical composition. An instrument of this type was first described in a paper by Etienne Louli in 1696, and Enbrayg (1732), Gabory (1771) and Harrison (1775) are also known to have made attempts at such devices. The first practical metronome was constructed in 1812 by Dutchman Dietrich Nikolaus Winkel. However, its invention is usually attributed to Johann Nepomuk Maelzel, of Ratisbon, who copied Winkel's design received a patent for the metronome in 1816.

The original metronome was a mechanical device consisted of a double pendulum with a sliding weight, the position of which is used to set the frequency of oscillation. It was modified in 1882 so that a click is produced on each swing of the pendulum rod, rather than being silent. Other approaches have included a clockwork metronome that produces a ticking sound on each beat until it runs down. Generally metronomes can be set to produce a certain number of beats per minute and it is important that the timing is reliable and regulated. Some metronomes may even produce two or more distinct sounds so that one sound indicates the beginning of each measure, and another indicates the beat within each measure.

Today, many metronomes are electronic with a dial or buttons used to set the tempo. Advantages over the classical spring-powered mechanical metronome are that they do not need to be rewound, and that they are easily portable. Also, some may include an LED that flashes on the beat, an adjustable volume control, and/or the generation of a tuning note. A note is generated by selecting the corresponding frequency, for example, the note A is the frequency 440Hz, C = 523Hz, D = 587Hz, F = 698Hz, G = 784Hz, A = 880Hz.

Theory/Design

Selection of Design

Every metronome requires a timing circuit. A simple metronome can be implemented using a 555 timer. The 555 timer is a very important and versatile chip in analogue electronics applications. For this reason, a metronome was chosen as a good example of

analogue electronics design. It is also a practical application that can be used by members of our group when pursuing musical endeavours.

To ensure that the metronome was functional and useable several design criteria were established:

- Precise selection of tempo
- Wide range of tempos
- Accuracy of output tempo
- Portable device
- Battery powered

Consideration of these design criteria highlighted the limitations of the 555 timer in implementing such a design. These include lack of precision in frequency selection, limited range of frequencies and attenuation of output signal due to frequency characteristics. For this reason other analogue timing and oscillator circuits were investigated. A crystal oscillator circuit was chosen to replace the 555 timer because of its precision.

Other metronomes on the market often have additional features such as a tone generator for tuning purposes. The possibility of adding such a function to the metronome was therefore researched. Due to the similarity in circuit design between a pitch generator and a metronome it is simple to include a selectable tone generator as part of the overall circuit.

Design Specifications

The following design specifications were generated for a metronome and pitch generator:

- Able to produce a short tone at a rate chosen by the user, range = 1 to 999 beats/minute
- Able to produce a constant tone at a pitch defined by the user, range = 1 to 999Hz
- Small portable device
- Able to be powered by a standard battery
- Able to produce sound loud enough to be heard above usual instrument sound

Block Diagram

The block diagram in Figure 1 shows the high level operation of the circuit. Each of these functional blocks is described in detail in the section on Operation of Circuit.

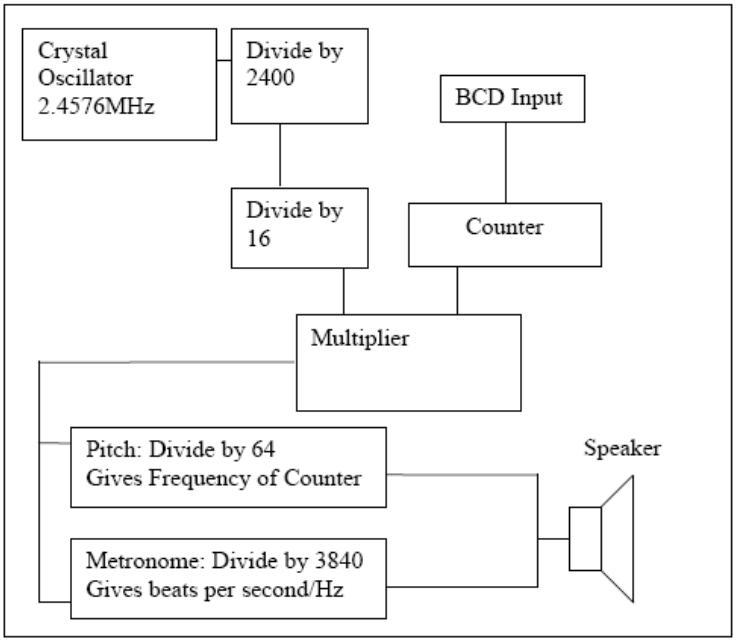

Figure 1: Block diagram of functional components in operation of the metronome and pitch generator circuit

Circuit Diagram

A detailed circuit diagram of the metronome and pitch generator is given in Figure 2. The components are listed in Table 1.

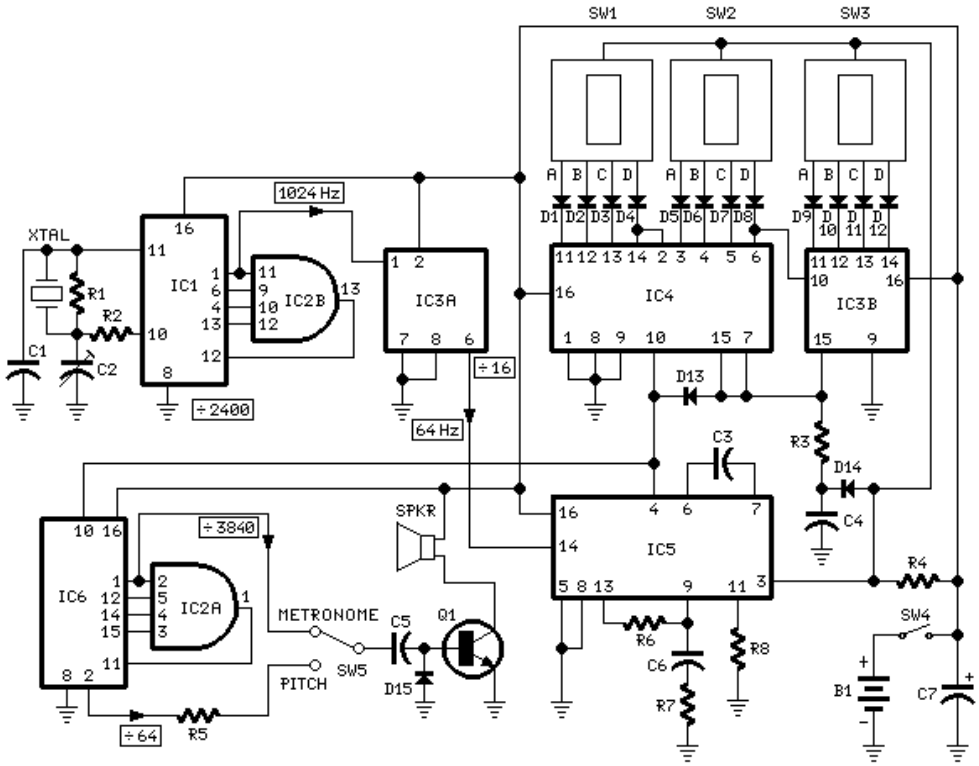

Figure 2: Circuit diagram for metronome and pitch generator circuit

Table 1 Component descriptions for metronome and pitch generator circuit

ID	Item	ID	Item
R1	1M 1/4W Resistor	IC1	4060 14 stage ripple counter and oscillator IC
R2	22K 1/4W Resistor	IC2	4082 Dual 4 input AND gate IC
R3	6K8 1/4W Resistor	IC3	4520 Dual binary up-counter IC
R4	4K7 1/4W Resistor	IC4	4518 Dual BCD up-counter IC
R5	47K 1/4W Resistor	IC5	4046 Micropower Phase-locked Loop IC
R6	100K 1/4W Resistor	IC6	4040 12 stage ripple counter IC
R7	39K 1/4W Resistor	Q1	BC337 45V 800mA NPN Transistor
R8	12K 1/4W Resistor	XTAL	2.4576 MHz Miniature Quartz crystal
C1	47pF 63V Ceramic Capacitor	SW1	BCD Miniature Thumbwheel Switch (1s)
C2	2-22pF 63V Ceramic Trimmer	SW2	BCD Miniature Thumbwheel Switch (10s)
C3	470pF 63V Ceramic Capacitor	SW3	BCD Miniature Thumbwheel Switch (100s)
C4	10pF 63V Ceramic Capacitor	SW4	SPST Slider Switch (On-off)
C5	100nF 63V Polyester Capacitor	SW5	SPDT Slider Switch (Metronome-Pitch)
C6	220nF 63V Polyester Capacitor	SPKR	8 Ohm, 50 mm. Loudspeaker
C7	22µF 25V Electrolytic Capacitor	B1	9V PP3 Battery
D1-D15	1N4148 75V 150mA Diodes	Clip	for 9V PP3 Battery

Operation of Circuit

Crystal Oscillator

The oscillator in IC1 (4060 14 stage ripple counter and oscillator IC) and the 2.4576 MHz crystal form a Pierce type oscillator circuit, a typical crystal oscillator circuit commonly used in microcontrollers. The circuit consists of two parts: 1) an inverting amplifier that supplies a voltage gain and 180° phase shift, and 2) a frequency selective feedback path. The feedback path contains a PI network formed by the crystal in combination with the capacitors C_1 and C_2 that stabilises the frequency and supplies a 180° phase shift in the feedback path. In steady state, the overall loop gain is unity and the overall phase shift is an integer multiple of 360°. The inverter is contained within the microcontroller and provides the 180° of phase shift necessary for oscillation.

The feedback resistor, R_1, is used to bias the input to the inverter. Only leakage current flows into the input of the inverter so there should be very little voltage drop across the feedback resistor, causing the input of the inverter to be pulled towards the voltage on the output. This unstable condition is necessary for oscillation. The value of R_1 affects the loop gain of the amplifier: reducing R_1 will reduce the loop gain while increasing it increases loop gain.

The series resistor, R_2, is used to limit the amount of drive current supplied to the crystal. The crystal is piezoelectric quartz which is able to provide extremely accurate timing. Crystals can be modelled as series R-L-C networks where R is the equivalent series resistance, C is the motional capacitance representing the elasticity of the quartz, and L is the motional inductance representing the vibrating mass of the crystal unit. The value of the series resistance must be sufficiently large to limit the current to crystal so that it is not overdriven and damaged. However, it must also be small enough so that oscillations can start quickly. If R_2 is too small the oscillations may start in unpredictable modes, but if it is too large oscillations will start slowly or not at all.

Part of the function of the bypass capacitors C_1 and C_2 is to create a low-pass filter. The capacitive load on one side of the crystal should be approximately equal to the capacitive load on the other side of the crystal, although C_1 may be greater than C_2 since the output capacitance of the inverter is usually slightly greater than the input capacitance. The capacitor C_2 is variable to allow the resonant frequency to be adjusted slightly.

Divide by 2400

The 14-stage ripple counter combined with the dual 4 input AND gate (IC2) provides division by 2400. This is because the ripple counter counts to 2400 ($2^{11}+2^8+2^6+2^5$, pins 1, 13, 6 and 4) each time before being reset by the output from the AND gate. Therefore the frequency is divided by 2400, reducing the frequency to 1024 Hz (2.4576 MHz/2400=1024Hz).

Divide by 16

IC3A (4520 Dual binary up-counter IC) provides further division by 16, delivering a 64 Hz stable frequency square wave. This is achieved by taking the highest bit (lowest frequency) output only from the counter.

Multiply by Counter Value

The 4046 micropower phase-locked loop (IC5) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The operation of a phase locked loop can be compared with automatic gain control – the difference is that PPL is for frequency whereas AGC is for voltage. The phase comparator of the phase locked loop compares two input signals and produces an error signal which is proportional to the difference between the frequencies of the inputs. This error signal drives a voltage-controlled oscillator (VCO), creating an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop as shown in Figure 3.

The error signal increases if the output frequency deviates from the desired value and drives the frequency in the opposite direction to reduce the error. The output frequency is therefore locked to the reference frequency. The circuit is able to generate multiple frequencies because of the divider placed between the output and the feedback input. For example, in this circuit the reference signal is 64 Hz and the divider can be preset to any value between 1 and 999. The error signal produced by the comparator will only be zero when the output of the divider is also 64Hz. For this to happen the VCO must operate at a frequency which is 64Hz times the divider count value. Therefore the output of the VCO will be 64Hz for a count of 1, 128Hz for a count of 2, and so on. The divider value is given by the number set on the three miniature BCD thumbwheel switches (units, tens and hundreds). Only whole multiples of the reference frequency can be obtained.

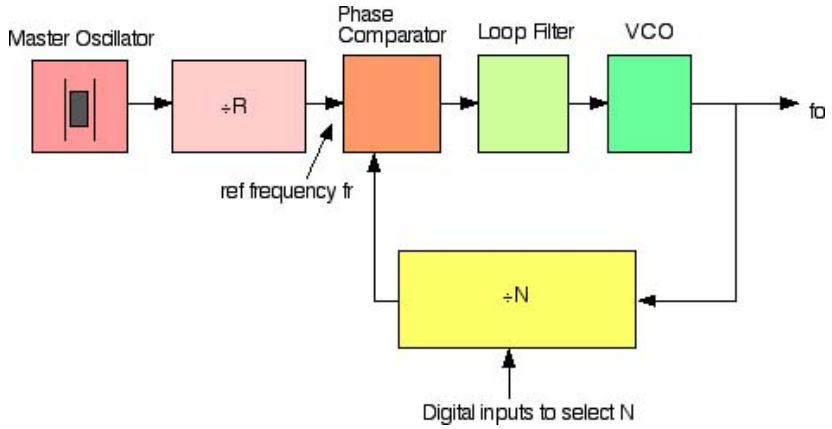

Figure 3: Operation of a phase locked loop frequency synthesiser (figure from http://en.wikipedia.org/wiki/Frequency_synthesiser)

The presence of the loop filter is necessary for practical implementation of a PPL. The loop filter is a low-pass filter placed between the output of the frequency comparator and the input of the VCO. This is because the input of the VCO must be DC voltage that is smooth and free from noise so that frequency modulation will not occur. The output of the frequency comparator is usually in the form of short error pulses and so requires filtering before being applied to the VCO. However, heavy filtering will make the VCO slow to respond to changes whereas light filtering will produce noise and other problems with harmonics. The design of the filter is therefore a very important part of the PPL system. In the metronome circuit the low pass filter is formed by the resistors R_6 and R_7 along with the capacitor C_6. The phase comparator and VCO are internal in the 4046 micropower phase-locked loop IC and the divide by N is the loop from pin 4 to pin 3 with inputs from IC4 and IC3.

Pitch Generator: Divide by 64

The output from the VCO is the input into IC6 (4040 12 stage ripple counter IC). Connecting the transistor base Q1 to pin 2 of IC6 via a switch (SW5), the frequency set by thumbwheel switches is obtained with quartz precision. This is because it is divided by 64 (by taking the output only from pin 2). Recall that the output from the VCO was 64 Hz times the divider count value (frequency set by the thumbwheel switches).

Therefore the division by 64 gives the value set on the thumbwheel switches as the output frequency. Volume regulation of the pitch generator is obtained trimming resistor R5.

Metronome: Divide by 3840

Similarly to the pitch generator, the output from the VCO is the input into IC6 (4040 12 stage ripple counter IC). However, in the ripple counter counts to 3840 ($2^{11}+2^{10}+2^9+2^8$, pins 1, 15, 14 and 12) each time before being reset by the output from the AND gate. Therefore the frequency is divided by 3840 before being applied to the base of the transistor Q1. This gives a the frequency set on the thumbwheel switches in beats per minute since the input was $64 \times \text{count}$ and the output is $\frac{64 \times \text{count}}{3840} = \frac{\text{count}}{60}$.

Implementation

PSPICE Simulation

Before constructing electronic circuits it is often a good idea to first simulate them using a computer program to test for correct operation and to gain a better understanding of the working of the circuit. PSPICE (Personal Simulation Program with Integrated Circuit Emphasis) is a software package that enables such simulations. The available version of PSPICE had a limited library of components and so did not contain all the ICs necessary to be able to simulate the crystal operated metronome. For this reason a simpler metronome circuit (Figure 4) was implemented in PSPICE that still allowed testing of the overall concept. This circuit operates using a 555 timer rather than a crystal oscillator so is not as reliable. In addition, the beats per minute value must be set by adjusting a linear potentiometer so the ease of use is reduced. There is also no pitch generator function.

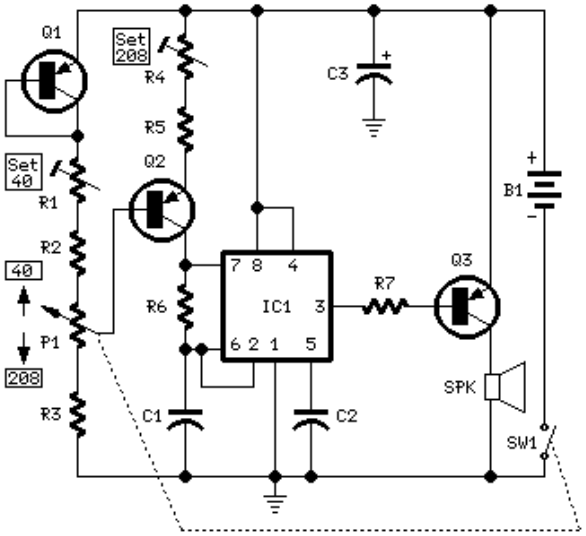

Figure 4: Simple metronome circuit using 555 timer

This circuit uses trimmer resistor to limit the device's range (R_1 lower limit and R_4 upper limit). It also uses a potentiometer (P_1) to control the range. The circuit has an operational range of 40 beats per minute (bpm) to 208 beats per minute. The

potentiometer is set in the simulation using a percentage to indicate how the device is divided: 0% is equivalent to the potentiometer pointing fully towards R_2 giving a value of 40bpm, and 100% is equivalent to the potentiometer pointing fully towards R_3 giving a value of 208bpm.

Breadboard

Components were purchased from Jaycar and the circuit constructed on a breadboard. A photograph of the functioning breadboard circuit is shown in Appendix A, Figure 6. IC2, the 4082 Dual 4 input AND gate IC, was not available so two 4012 Dual 4 input NAND gate ICs were used instead. One NAND gate in each IC was used as a NAND gate and the other one was used to invert this signal to give the same output as an AND gate.

Initially, the circuit operation was verified using a function generator instead of the crystal oscillator circuit as no oscillations were occurring. Researching the operation of crystal oscillator circuits showed that oscillations will not start if the value of the series resistor, R_2, is too large. The choice of R_2 is largely dependent on the particular crystal used, but no information on the crystal was available from the manufacturer. The value of R_2 was repositioned (see Figure 5) to agree with typical crystal oscillator circuit configurations and gradually reduced from its original value of 22kΩ . The circuit began to just operate at a value of R_2=3.3 kΩ. A value of 2.2 kΩ (10 times less than the original) was chosen for the final implementation to ensure that R_2 was not too high or too low. This agrees with the Philips Semiconductor data sheet for 4060 14 stage ripple counter and oscillator IC which suggested a typical value for R_2 of 2.2kΩ.

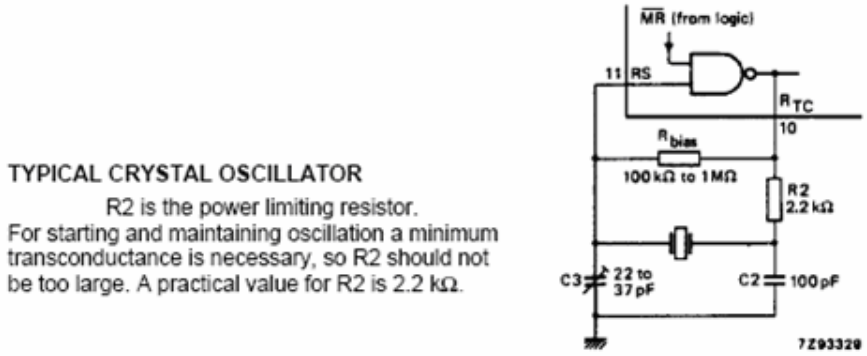

Figure 5: A typical crystal oscillator circuit showing the positioning of the resistors and capacitors relative to the crystal (figure from 74HC/HCT4060 14-stage binary ripple counter with oscillator, *Philips Semiconductors,* December 1990.)

EAGLE PCB

After testing and finetuning the circuit in the breadboard implementation a printed circuit board was designed using EAGLE. The first stage involved constructing a schematic of the circuit which is shown in Appendix D: EAGLE PCB Layout Design Figure 14.

There are a few changes from the original and breadboard circuits. The resistor R_2 was moved into series with the crystal and in parallel with R_1. On the bread board implementation two dual 4-input NAND gates were used instead of one dual 4-input

AND gate due to component's availability, however a 4082 Dual 4 input AND gate IC should be acquired for the final PCB circuit.

The circuit was straight forward to construct in EAGLE. However, the program contained a very large library of components and finding the exact ones proved difficult and time consuming. In some cases unequivocal identification was not possible so the closest match was used. Validation of the choices will not be possible until the final PCB is constructed. No earth function was available, so all the earth wires needed to be connected together to ensure that the current path was complete.

Once the circuit schematic was complete, the program was used to convert this to a Printed Circuit Board design. This created a board and placed all the components with their connections off to one side. Placing the components on the board proved very difficult, as creating some semblance of order, flow and continuity took a lot of time and effort. In the end a workable and seemingly ordered PCB board was produced. All that was then required was to ensure that the power pins (16) and the earth pins (8) on all the integrated circuits were connected to the correct place. The program did not allow these pins to be connected up in the circuit schematic and when converted to a board only connected all the pin 16's from the ICs to each other but not to the power supply, and similarly for the earths on the pin 8's.

After this was fixed the board design was checked by Ian McRobert, who said it was good and reasonably clean. He did note that some of the lines may need to be widened and said that he would look in to it and fix it. The board design that went to Ian before being sent to BEC for manufacturing is given in Appendix D: EAGLE PCB Layout Design Figure 15.

Results

PSPICE Simulation

The spikes in the output voltage at the speaker indicate the beats of the metronome and they occur at the expected intervals. For example 90bpm is one beat every two thirds of a second (T=0.666s) with potentiometer set at 34.35% and 120bpm is one beat every half a second (T=0.5s) with potentiometer set at 51%. The output graphs are shown in Appendix B: PSPICE Implementation Figure 8 and Figure 9, respectively.

Setting of an exact beats per minute value for this circuit in simulation requires calculation of the percentage value for the potentiometer setting. However, this becomes more difficult in a practical implementation of the circuit, where the potentiometer scale setting would have to be marked with a pen while comparing the output to that of another metronome. This is an imprecise method and may give inaccurate values for the output of the device. Another inaccuracy is that the values of R1 and R4 are set to place upper and lower limits on the output range of the device so the output is dependent on these values. It was recommended that the exact upper and lower limits be established using another metronome. The setting could be done using a CRO for greater accuracy, however using this every time you what to change the speed is impractical.

This model shows the inaccuracies of using hand tuned devices for a metronome circuit. However, it does demonstrate the correct operation of a metronome circuit and clearly shows the expected outputs. The crystal operated circuit should overcome the limitations of this simple metronome circuit as allows for precise setting of output beats per minute over a range of 1 to 999.

Breadboard

The operation of the metronome and pitch generator was verified using a digital oscilloscope. A sample of the outputs is shown in Appendix C: Breadboard Results Figure 10-Figure 13. When the metronome was set to 90 beats per minute the beats are clearly visible at a frequency of 1.515 Hz. This is equivalent to $60\,\text{sec}/\,\text{min}\times f = 60\,\text{sec}/\,\text{min}\times 1.515\,Hz = 90.9/\,\text{min}$. The measured value of 90.9 beats per minute (Figure 10) is very close to the expected value of 90 beats per minute. Similarly, when the metronome was set to 120 beats per minute the beats are clearly visible at a frequency of 2.02 Hz (Figure 11) which is equivalent to $60\,\text{sec}/\,\text{min}\times f = 60\,\text{sec}/\,\text{min}\times 2.02\,Hz = 121.2/\,\text{min}$. Again the measured and expected values show good agreement. Comparing these outputs with those from the PSPICE simulation shows that there is some noise in the practical circuit, especially along the baseline. However, the peaks (spikes) in the output look similar and the main consideration is that the beats themselves are easily distinguishable and reasonably clean.

In the case of the pitch generator the frequency was set to 440Hz which is an octave 4 A and 880 Hz, an octave 5 A. The resulting outputs were at 440.5 Hz and 881 Hz respectively as can be seen in Figure 12 and Figure 13. There is therefore good agreement between the measured and expected values.

EAGLE PCB

Due to time constraints arising from the late ordering and arrival of the PCB no results are available at this time.

Conclusion

A functional metronome and pitch generator circuit was implemented successfully. The breadboard implementation met the established design criteria for a metronome: precise selection of tempo was possible across a wide range of tempos with accurate output. Also, the pitch generator function made the circuit more practical and useful. To make the circuit more useable and portable a printed circuit board was designed, manufactured and constructed. The implementation took a circuit from schematic through electronic simulation, breadboarding and troubleshooting, to a printed circuit board that could be used in a real world application. Through this process valuable skills in the theoretical and technical sides of analogue electronics were honed and attained.

References

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16. HEF4518B MSI Dual BCD counter, *Philips Semiconductors,* January 1995.
17. HEF4520B MSI Dual binary counter, *Philips Semiconductors,* January 1995.

Appendix A: Photograph of Circuit

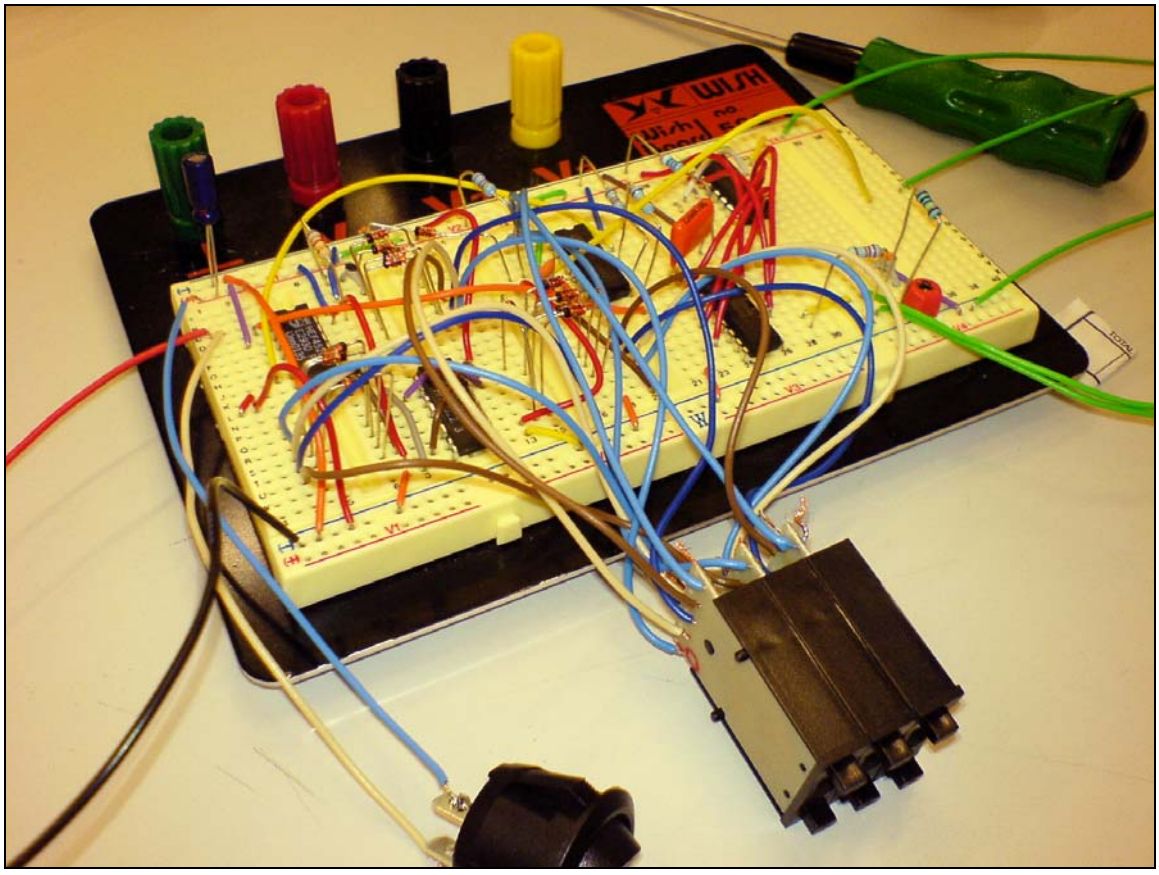

Figure 6: Photograph of breadboard circuit

Appendix B: PSPICE Implementation

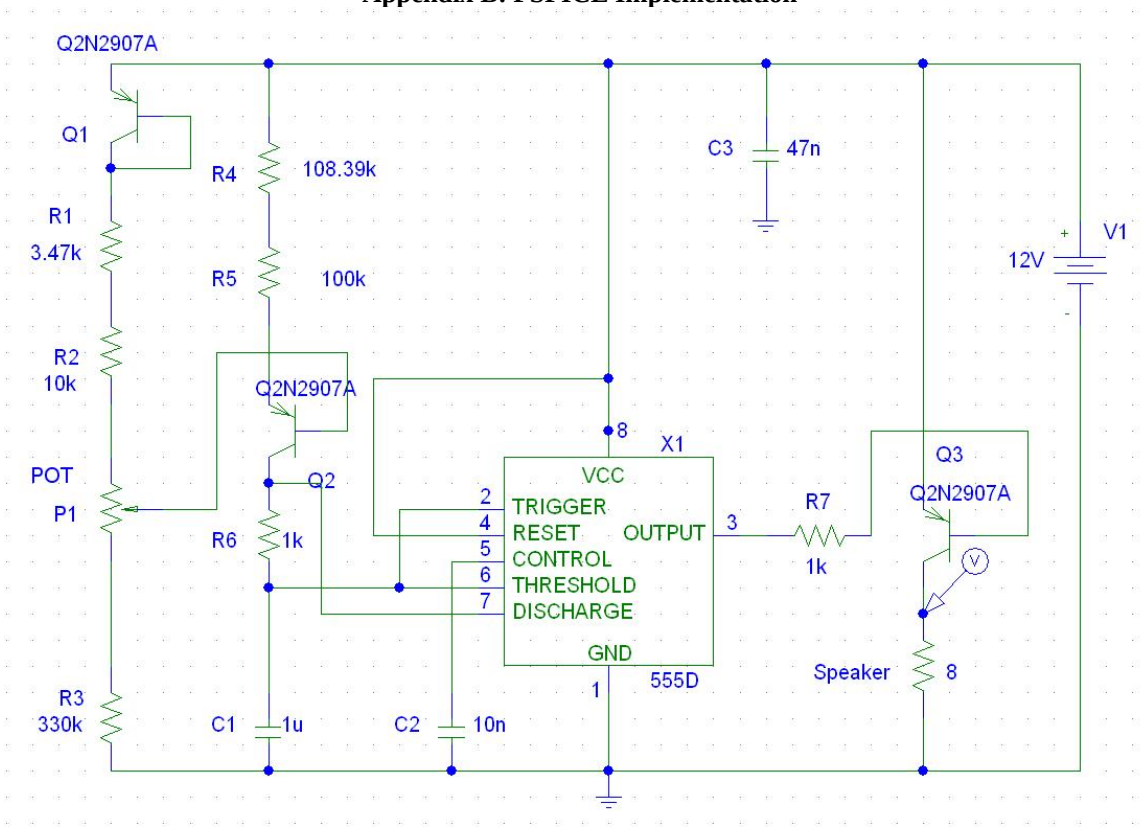

Figure 7: PSPICE schematic of simple metronome using 555 timer

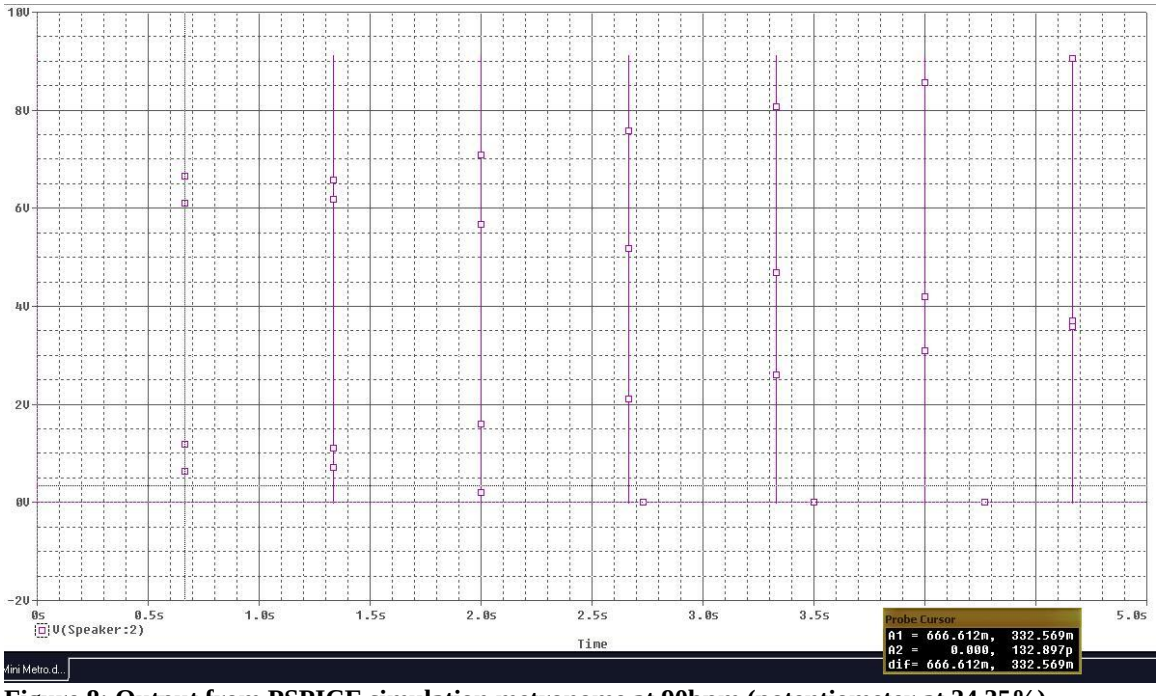

Figure 8: Output from PSPICE simulation metronome at 90bpm (potentiometer at 34.35%)

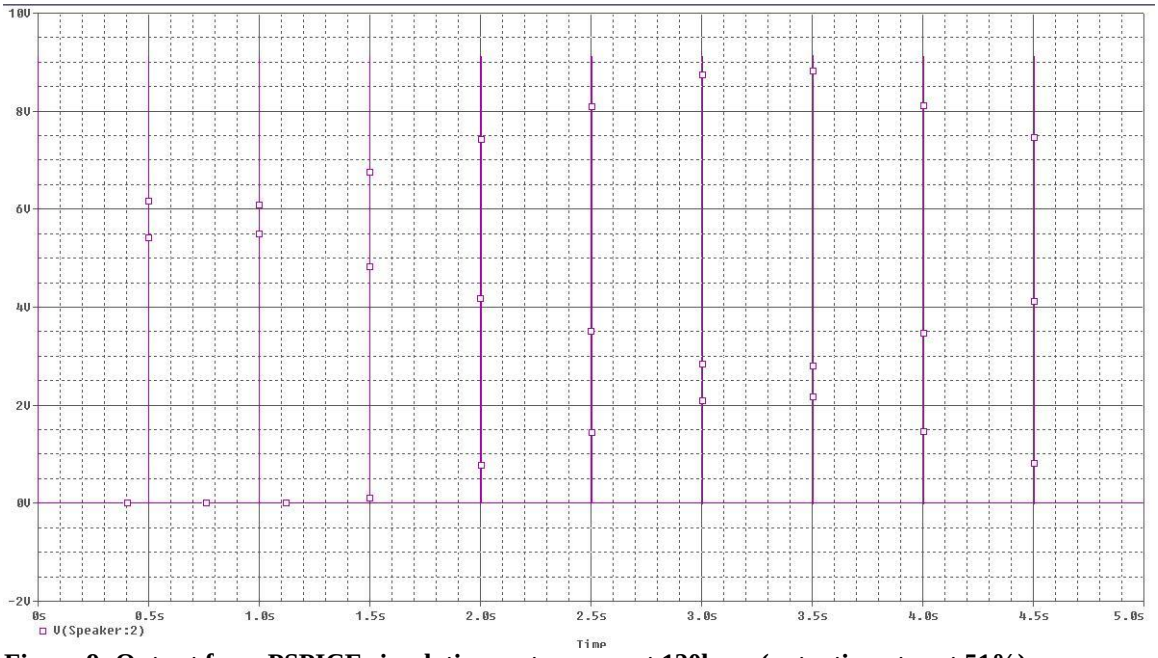

Figure 9: Output from PSPICE simulation metronome at 120bpm (potentiometer at 51%)

Appendix C: Breadboard Results

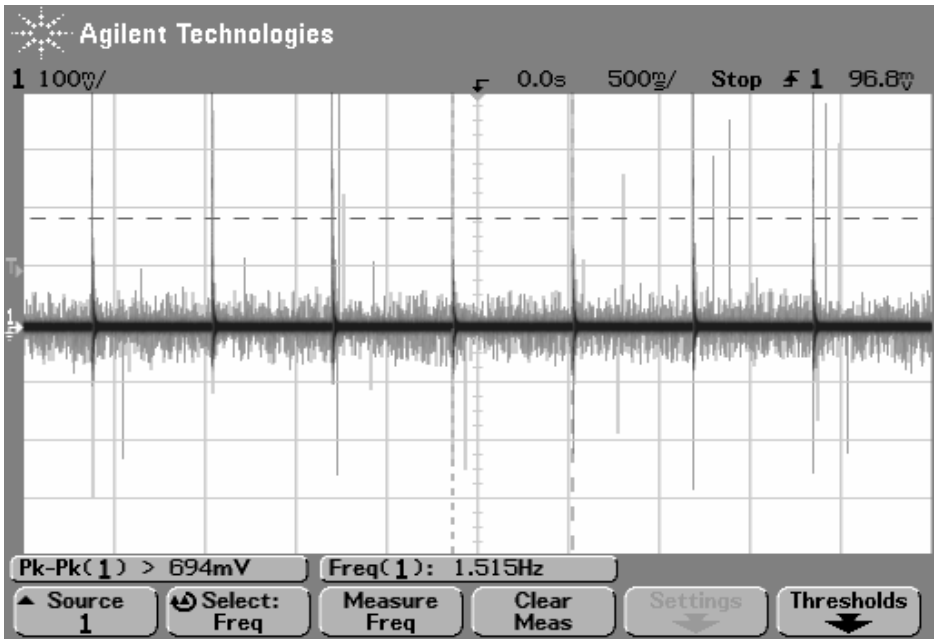

Figure 10: Output from breadboard implementation with crystal oscillator metronome set at 90 beats per minute

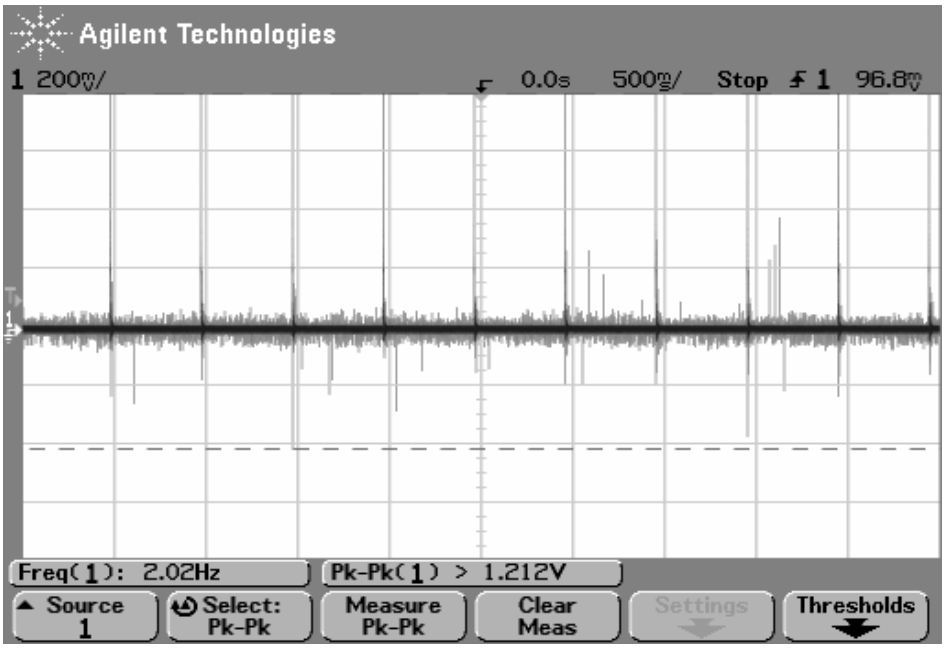

Figure 11: Output from breadboard implementation with crystal oscillator metronome set at 120 beats per minute

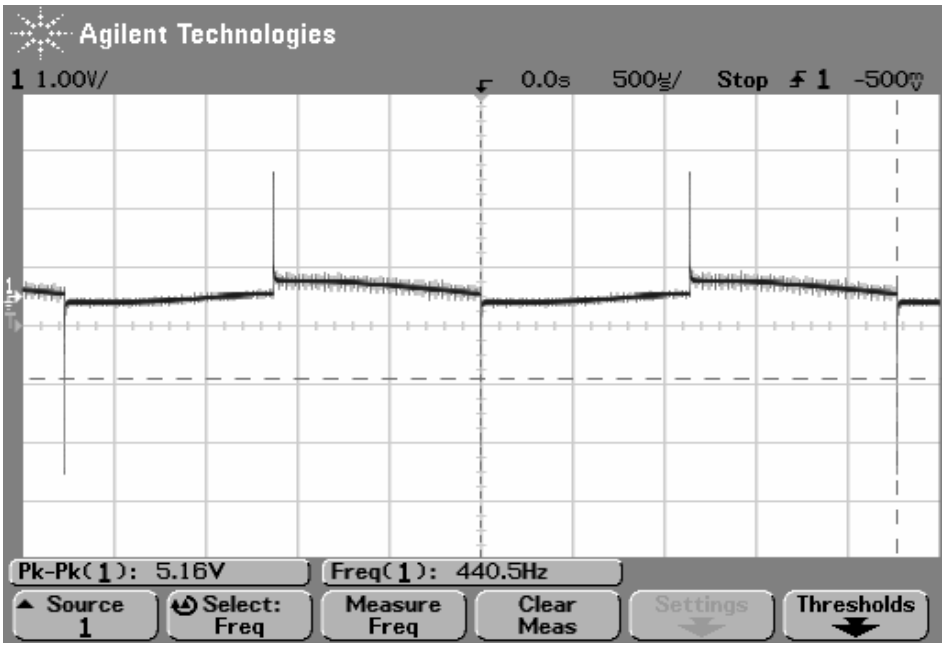

Figure 12: Output from breadboard implementation with crystal oscillator pitch generator set at 440Hz

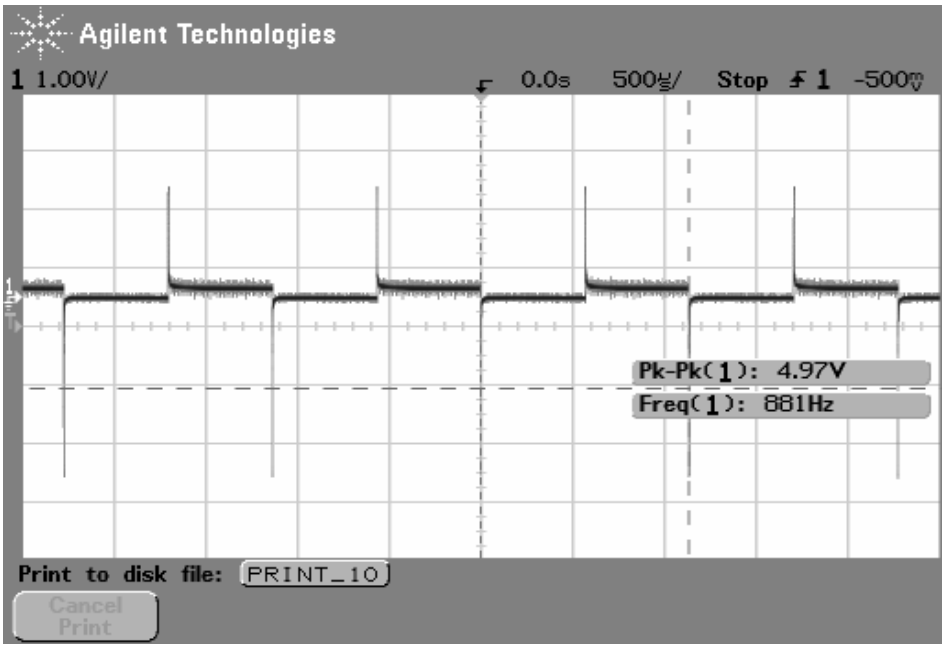

Figure 13: Output from breadboard implementation with crystal oscillator pitch generator set at 880Hz

Appendix D: EAGLE PCB Layout Design

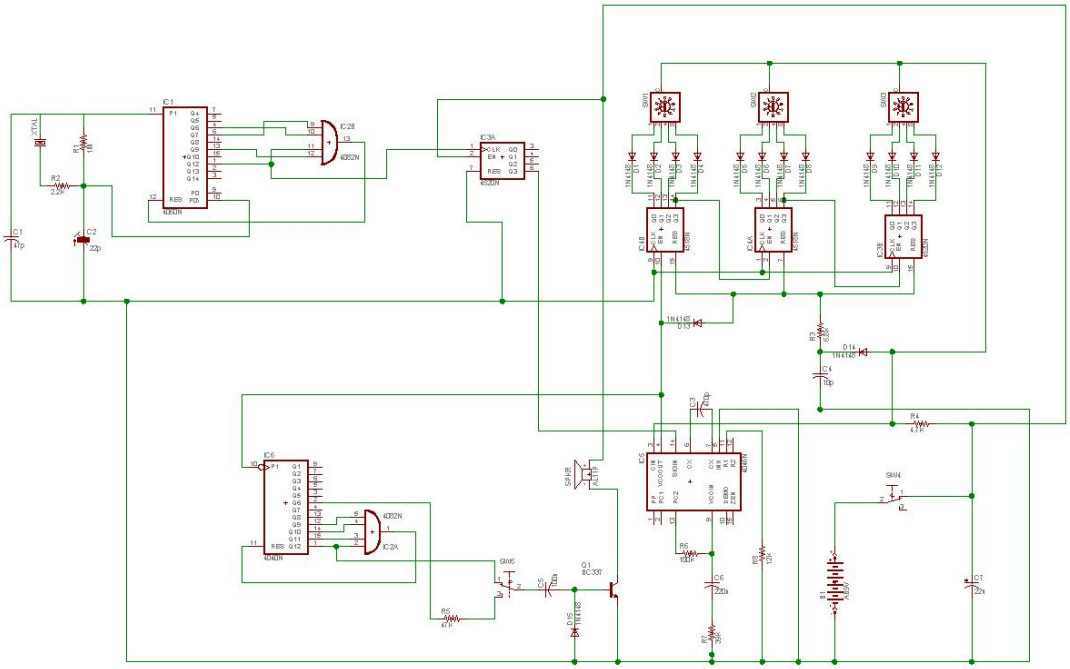

Figure 14: Schematic of metronome and pitch generator circuit for PCB design

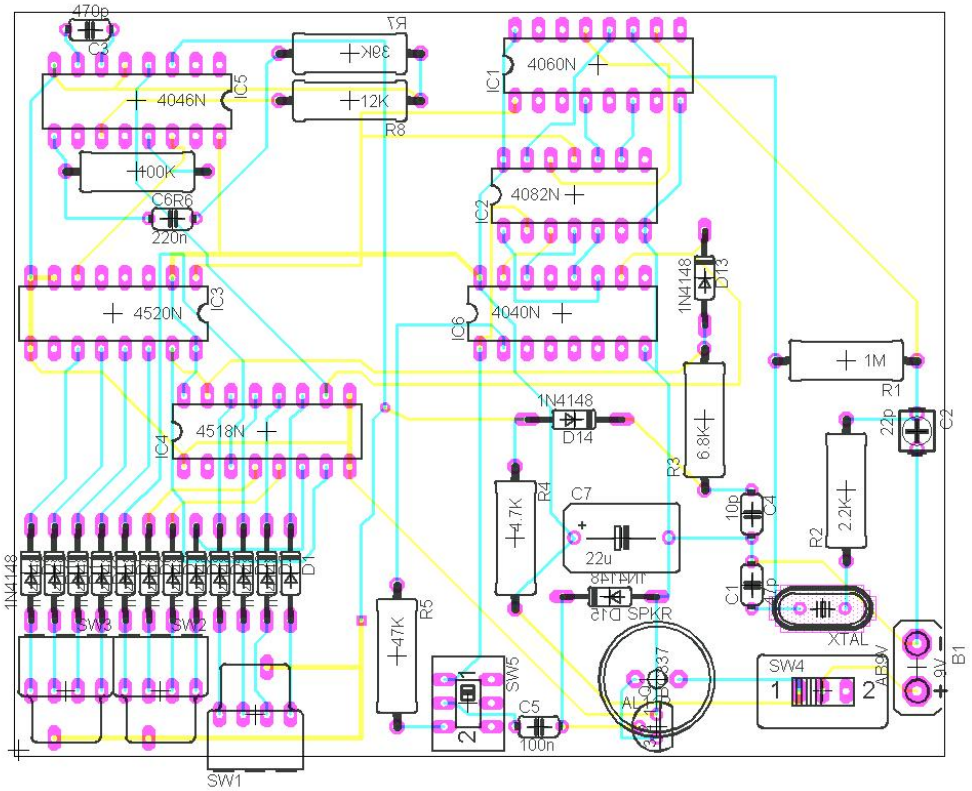

Figure 15: PCB Layout design for metronome and pitch generator circuit